

Series PA7

7.0 x 5.0 mm SMD Analog Frequency Multiplier Differential Output Voltage Controlled Crystal Oscillator

FEATURE

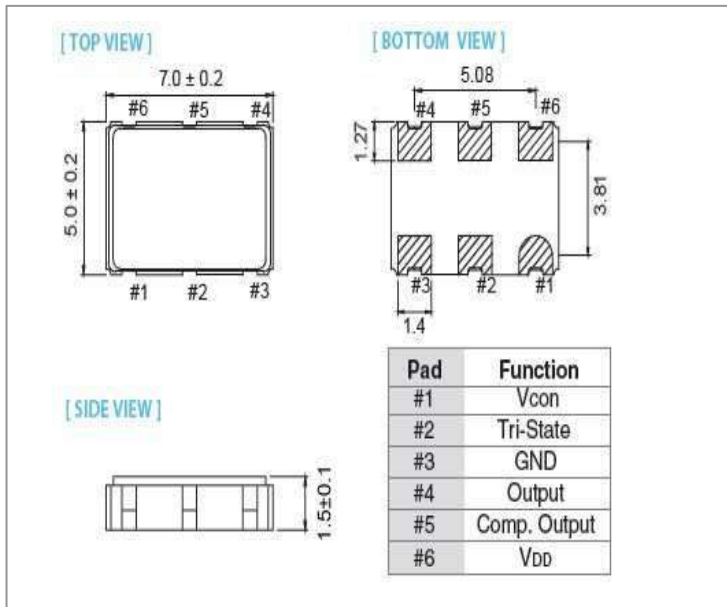
- Typical 7.0 x 5.0 x 1.5 mm hermetically sealed ceramic package.
- Very low jitter performance < 0.1 pS RMS from 12k-20MHz.
- Wide frequency control range.
- Output frequency up to 800 MHz.
- Tri-state enable/disable.
- LVPECL output.



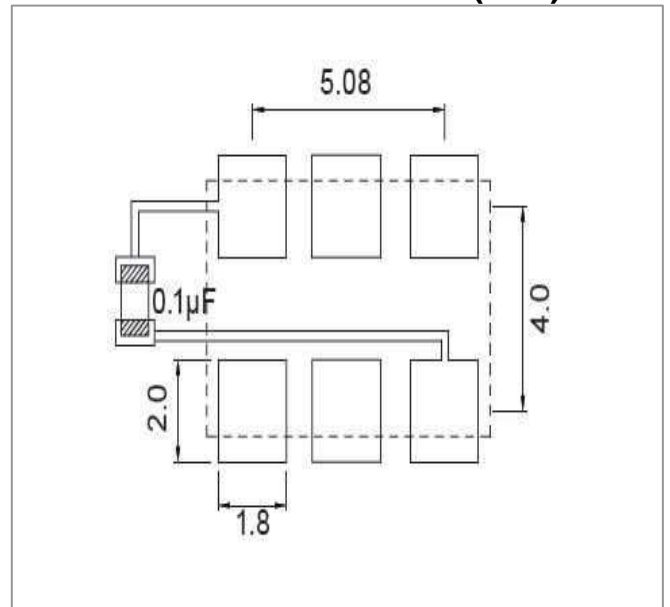
TYPICAL APPLICATION

- Telecommunications such as SONET / SDH / DWDM / FEC / SERDES / OC-3 thru OC-192
- Wireless base stations / WLAN / Gigabit Ethernet
- Clock and Data Recovery
- Low Jitter Clock Generation
- Avionic Flight Controls

DIMENSION



SOLDER PAD LAYOUT (mm)



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ELECTRICAL SPECIFICATION

Parameter	PECL		Unit
	3.3V		
	Min.	Max.	
Supply Voltage Variation (VDD) 5%	3.135	3.465	V
Frequency Range	120	800	Mhz
Standard Frequency	245.76, 491.52, 614.4, 622.08		
Absolute Pulling Range (APR)	±50	-	ppm
Control Voltage Range	0.3	3	V
Supply Current 120MHz ≤ F0 ≤ 800MHz	-	100	mA
Output Level Output High (Logic "1")	2.275	-	V
Output Low (Logic "0")	-	1.68	
Transition Time: Rise/Fall Time	-	1.0	nSec
Start Time	-	3.0	mSec
Tri-State (input to Pin 2)			
Enable (High voltage or floating)	0.7VDD	-	V
Disable (Low voltage or GND)	-	0.3VDD	
Linearity		10	%
Modulation Bandwidth (BW)	40	-	KHz
Inut Impedance	130	-	KΩ
RMS Phase Jitter integrated 12KHz ~ 20MHz (622.08MHz)		0.1	pSec
50KHz ~ 80MHz (622.08MHz)	-	0.15	
Phase Noise (622.08MHz) 100 Hz	-	-70	dBc/Hz
1 KHz	-	-100	
10 KHz	-	-120	
Aging	-	±3	ppm
Storage Temp. Range	-55	125	°C

Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.

Transition times are measured between 20% and 80% of VDD Packing:

Tape & Reel, 1000pcs per Reel.

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FREQ. STABILITY vs TEMP. RANGR

Tem.(°C) \ ppb	±25	±50
-10 ~+60	O	O
-20 ~+70	Δ	O
-40 ~+85	×	O

O: Available Δ:Conditional X: Not available
 Inclusive of calibration@25°C,operating temperature range, input voltage variation,
 load variation, aging(1st year),shock, and vibration