



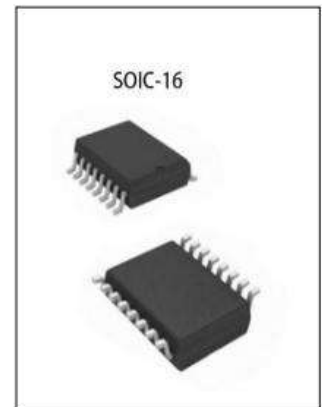
## Quad-Channel Digital Isolators

### CYP584X

#### General Description

CYP584X series is a Quad-channel digital isolator, using Chip level high voltage isolation process, isolation voltage up to 5KVrms. This series of products have low radiation, excellent anti-electromagnetic interference performance, high transmission rate and low power consumption; Equipped with enable pins to place the output in a high impedance state.

It has fail-safe mode, which can restore the output to the default state when the input power loss. This series of products have 4 in 0 out, 3 in 1 out, 2 in 2 out and other specifications, the specific product information, see the product selection table.



#### Features

- High data rate: 150Mbps
- Wide supply voltage range: 2.5V~5.5V
- Isolation withstand voltage: 5KVrms
- Wide temperature range: -40°C~125°C
- Low power consumption: 1.5mA/ch (1Mbps)
- Low propagation delay: 11ns (typ.)
- High CMIT: 50 KV/us
- Isolation barrier life: >40 years
- PB-free and ROHS compliant models available
- SOIC-16 package
- ESD: HBM  $\pm 8KV$ , MM  $\pm 400V$

#### Applications

- Industrial automation system
- Medical equipment
- Automotive electronics
- New energy
- Motor control

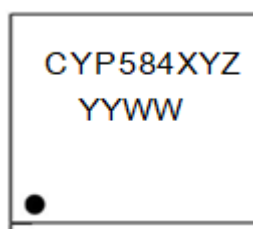


## Order specification

### Selection Table

Part No	The total number of channels	Number of reverse channels	Default output level	Package	Manner of Packing	Devices per reel
CYP5840ED	4	0	High	SOIC-16	Reel	2000
CYP5841ED	4	1	High	SOIC-16	Reel	2000
CYP5842ED	4	2	High	SOIC-16	Reel	2000
CYP5845ED	4	0	High	SOIC-16	Reel	2000
CYP5840BD	4	0	Low	SOIC-16	Reel	2000
CYP5841BD	4	1	Low	SOIC-16	Reel	2000
CYP5842BD	4	2	Low	SOIC-16	Reel	2000
CYP5845BD	4	0	Low	SOIC-16	Reel	2000

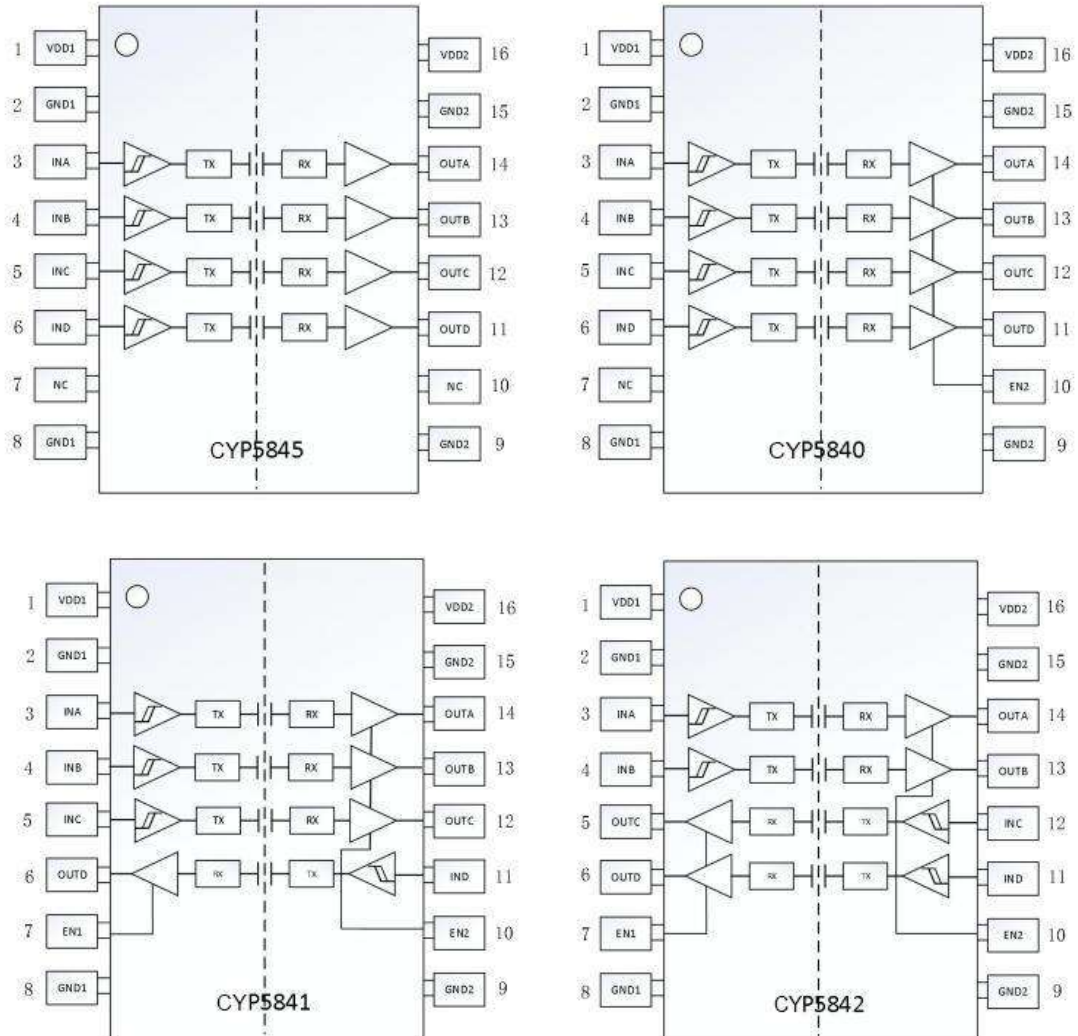
### Vertical View



### Definition of Marking

First line marking	Production serial Number	CYP584XYZ: Quad-channel digital isolator X indicates the number of reverse channels, 5/0:no reverse channel; 2:two reverse channels; 1:one reverse channels. Y indicates the default output status, B:The default output is low; E:The default output is high. Z indicates isolation voltage, A=1KV; B=2.5 KV; C=3.75 KV; D=5KV.
Second line marking	Production batch number	YY=years; WW=weeks.

**Block Diagram and Pin Arrangement Diagram**



**Pin Assignment****CYP5840/5845**

Pin No.	Pin Name	Description
1	VDD1	Supply voltage 1
2	GND1	Ground 1
3	INA	Digital signal input channel A
4	INB	Digital signal input channel B
5	INC	Digital signal input channel C
6	IND	Digital signal input channel D
7	NC	-
8	GND1	Ground 1
9	GND2	Ground 2
10	EN2/NC	CYP5840 is output enable pin 2, high level is valid, default high level. CYP5845 is NC. Enabled by default.
11	OUTD	Digital signal output channel D
12	OUTC	Digital signal output channel C
13	OUTB	Digital signal output channel B
14	OUTA	Digital signal output channel A
15	GND2	Ground 2
16	VDD2	Supply voltage 2

**CYP5841**

Pin No.	Pin Name	Description
1	VDD1	Supply voltage 1
2	GND1	Ground 1
3	INA	Digital signal input channel A
4	INB	Digital signal input channel B
5	INC	Digital signal input channel C
6	OUTD	Digital signal output channel D
7	EN1	Output enable pin 1, high level is valid, default high level.
8	GND1	Ground 1
9	GND2	Ground 2



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10	EN2	Output enable pin 2, high level is valid, default high level.
11	IND	Digital signal input channel D
12	OUTC	Digital signal output channel C
13	OUTB	Digital signal output channel B
14	OUTA	Digital signal output channel A
15	GND2	Ground 2
16	VDD2	Supply voltage 2

## CYP5842

Pin No.	Pin Name	Description
1	VDD1	Supply voltage 1
2	GND1	Ground 1
3	INA	Digital signal input channel A
4	INB	Digital signal input channel B
5	OUTC	Digital signal output channel C
6	OUTD	Digital signal output channel D
7	EN1	Output enable pin 1, high level is valid, default high level.
8	GND1	Ground 1
9	GND2	Ground 2
10	EN2	Output enable pin 2, high level is valid, default high level.
11	IND	Digital signal input channel D
12	INC	Digital signal input channel C
13	OUTB	Digital signal output channel B
14	OUTA	Digital signal output channel A
15	GND2	Ground 2
16	VDD2	Supply voltage 2

**Absolute Maximum Ratings(1)**

Unless specified otherwise, Tamb= 25°C

Parameter	Symbol	Value	Unit
Supply Voltage	VDD1/VDD2	-0.5~6	V
A/B Input Voltage	V <sub>INA</sub> /V <sub>INB</sub>	-0.5~VDD1/VDD2+0.5 <sup>(2)</sup>	V
Operating Temperature	T <sub>amb</sub>	-40~125	°C
Junction Temperature	T <sub>J</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-65~150	°C
Pin Temperature(reflow soldering)		260	°C
Rated Insulation with Stand Voltage		5	KVrms <sup>(3)</sup>

Note: (1) If the operating conditions exceed the above "Absolute Maximum Ratings", it may cause permanent damage to the device. The above values are only maximum values for operating conditions and we do not recommend devices to operate outside this specification. The stability of devices may be affected under absolute limit parameter conditions for a long time.

- (2) The maximum input voltage cannot exceed 6V.
- (3) Test instructions: Insulation for

**Recommended Operating Range**

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Temperature	T <sub>A</sub>	-40	25	125	°C
Supply Voltage	VDD1	2.5	-	5.5	V
Supply Voltage	VDD2	2.5	-	5.5	V

**DC Electrical Characteristics**

Unless specified otherwise, VDD=2.5V 5% or 3.3V 10% or 5V 10%, Tamb=25°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Undervoltage threshold	VDD <sub>UV+</sub>	VDD1, VDD2 rising up	1.9	2.2	2.37	V
VDD Undervoltage threshold	VDD <sub>UV-</sub>	VDD1, VDD2 failing down	1.85	2.12	2.32	V
VDD Undervoltage hysteresis	VDD <sub>HYS</sub>		50	70	95	mV
Positive input threshold	V <sub>T+</sub>	All inputs rising up	1.4	1.6	1.9	V
Reverse input threshold	V <sub>T-</sub>	All inputs failing down	1.0	1.3	1.4	V
Input Threshold Hysteresis	V <sub>HYS</sub>		0.38	0.44	0.50	V



## CYP584X

High Level Input Voltage	$V_{IH}$		2.0	–	–	V
Low Level Input Voltage	$V_{IL}$		–	–	0.8	V
High Level Output Voltage	$V_{OH}$	$I_{OH}=-4mA$	VDD -0.4	VDD -0.2	–	V
Low Level Output Voltage	$V_{OL}$	$I_{OL}=4mA$	–	0.2	0.4	V
Input leakage current	$I_L$		–	–	$\pm 10$	$\mu A$
Output Impedance <sup>(1)</sup>	$Z_O$		–	50	–	$\Omega$
Enable input current	$I_{ENH}, I_{ENL}$	$V_{EN}=V_{IH}$ or $V_{IL}$	–	2.0	–	$\mu A$
Data Rate			0	–	150	Mbps
Minimum Pulse Width			–	–	5.0	ns
Propagation Delay	$t_{PHL}, t_{PLH}$	See Figure 2	5.0	9.0	15	ns
Pulse Width Distortion $ t_{PLH}-t_{PHL} $	PWD	See Figure 2	–	0.2	4.5	ns
Part-to-Part Delay Skew <sup>(2)</sup>	$t_{PSK(P-P)}$		–	2.0	4.5	ns
Channel-to-Channel Delay Skew	$t_{PSK}$		–	0.4	2.5	ns
Rising Time	$t_r$	$CL=15pF$ , See Figure 2	–	2.2	4.0	ns
Falling Time	$t_f$	$CL=15pF$ , See Figure 2	–	2.2	4.0	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$		–	350	–	ps
Common Mode Transient Immunity	CMTI	$V_I=V_{DD}$ or 0 $V_{CM}=1500V$	35	50	–	$kV/\mu s$

Enable to Data high Valid	$t_{en1}$	See Figure 1	–	5.0	12	ns
Disable high to Tri-State	$t_{en2}$	See Figure 1	–	65	98	us
Input Drop Time to Effective Output Drop Time	$t_{SD}$		–	28	45	ns
Startup Time <sup>(3)</sup>	$t_{SU}$		–	15	45	$\mu s$

Note: (1) The nominal output impedance of the isolator channel is approximately  $50\Omega \pm 40\%$ , which is a combination of on-chip series resistors and output FET channel resistors. When driving load, transmission line effect will be a factor affecting the signal, the output pin should be connected to impedance controlled PCB wiring.

(2) TPSK(P-P) is the magnitude of the difference in propagation delay time measured between different units operating at the same supply voltage, load, and ambient temperature.

(3) The startup time is the time between the power supply and the output of valid data.

## Operating principle

Output status vs. power status

VDD1 status	VDD2 status	Input	Output	Comment
P	P	H	H	Normal operation.
P	P	L	L	
P	P	X	Hi-Z	Output Disabled, the output is high impedance
UP	P	X	L H	Failsafe mode, the output is default. When the input power is powered on again, the signal output responds synchronously with the signal input within 1us.
UP	P	X	Hi-Z	Output Disabled, the output is high impedance
P	UP	X	-	When the power supply of the output terminal is powered on again, EN=H or NC, the signal output terminal recovers the synchronous response of the signal input terminal within 1us. EN=L, the signal output end restores to high resistance state within 1us.

Note: 1.X=indeterminate; H=logic high; L=logic low; Hi-z=high resistance state.

2.P indicates the power-on status ( $2.5 < VDD < 5.5$ ); UP indicates the power failure state (VDD=0).

Enable process timing

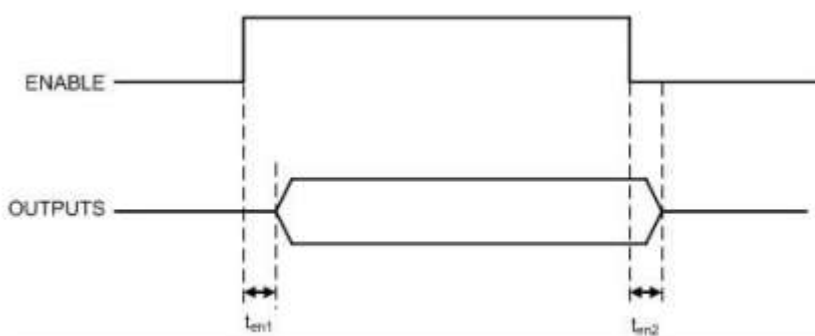


Figure 1

Parameter	Symbol	Min	Typ	Max	Unit
Enable to Data high Valid	$t_{en1}$	-	5.0	12	ns
Disable high to Tri-State	$t_{en2}$	-	65	98	us



Transmission delay

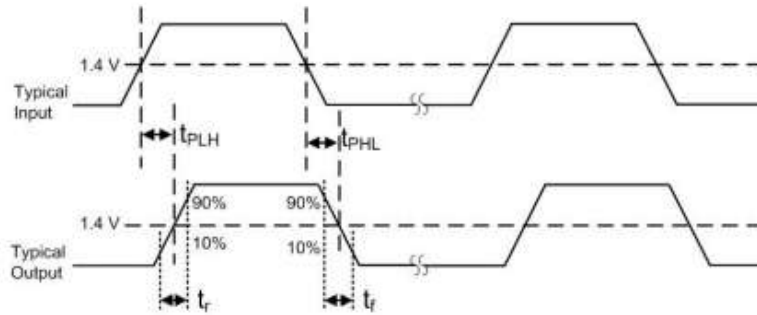
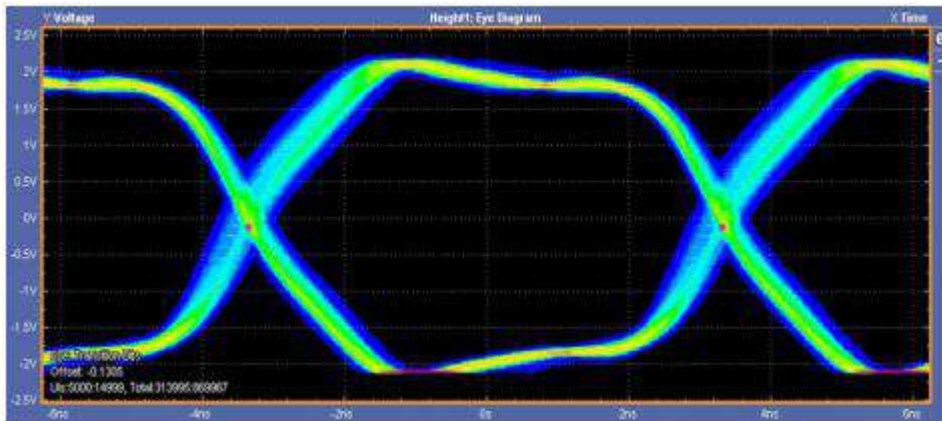


Figure 2

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay	$t_{PHL}, t_{PLH}$		5.0	9.0	15	ns
Pulse Width Distortion [ $t_{PLH} - t_{PHL}$ ]	PWD		–	0.2	4.5	ns
Rising Time	$t_r$	CL=15pF	–	2.2	4.0	ns
Falling Time	$t_f$	CL=15pF	–	2.2	4.0	ns

Eye Diagram





### DC Supply Current

VDD=2.5V 5% or 3.3V 10% or 5V 10%, Tamb= 40~125°C

Part No	Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
CYP5840/5Bx, Ex	V <sub>DD1</sub>	Power Supply 1	VI = 0(Bx), 1(Ex)	–	1.1	1.7	mA
	V <sub>DD2</sub>	Power Supply 2	VI = 0(Bx), 1(Ex)	–	2.5	3.8	
	V <sub>DD1</sub>	Power Supply 1	VI = 1(Bx), 0(Ex)	–	6.2	9.4	
	V <sub>DD2</sub>	Power Supply 2	VI = 1(Bx), 0(Ex)	–	2.6	4.2	
CYP5841Bx, Ex	V <sub>DD1</sub>	Power Supply 1	VI = 0(Bx), 1(Ex)	–	1.5	2.3	mA
	V <sub>DD2</sub>	Power Supply 2	VI = 0(Bx), 1(Ex)	–	2.5	3.8	
	V <sub>DD1</sub>	Power Supply 1	VI = 1(Bx), 0(Ex)	–	5.2	7.8	
	V <sub>DD2</sub>	Power Supply 2	VI = 1(Bx), 0(Ex)	–	3.7	5.5	
CYP5842Bx, Ex	V <sub>DD1</sub>	Power Supply 1	VI = 0(Bx), 1(Ex)	–	1.5	3.0	mA
	V <sub>DD2</sub>	Power Supply 2	VI = 0(Bx), 1(Ex)	–	1.5	3.0	
	V <sub>DD1</sub>	Power Supply 1	VI = 1(Bx), 0(Ex)	–	5.0	6.8	
	V <sub>DD2</sub>	Power Supply 2	VI = 1(Bx), 0(Ex)	–	5.0	6.8	

### AC Supply Current

VDD=5V 10%, Tamb= 40~125°C



## CYP584X

Part No	Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit		
CYP5840/5Bx, Ex	V <sub>DD1</sub>	Power Supply 1	1Mbps Power supply current (all inputs with 500 kHz rectangular wave , all outputs with CL=15pF)	-	4.2	5.5	mA		
	V <sub>DD2</sub>	Power Supply 2		-	2.5	4.1			
CYP5841Bx, Ex	V <sub>DD1</sub>	Power Supply 1		10Mbps Power supply current (all inputs with 5MHz rectangular wave , all outputs with CL=15pF)	-	3.5	4.9	mA	
	V <sub>DD2</sub>	Power Supply 2			-	3.1	4.7		
CYP5842Bx, Ex	V <sub>DD1</sub>	Power Supply 1			100Mbps Power supply current (all inputs with 50MHz rectangular wave , all outputs with CL=15pF)	-	3.5	4.8	mA
	V <sub>DD2</sub>	Power Supply 2				-	3.5	4.8	
CYP5840/5Bx, Ex	V <sub>DD1</sub>	Power Supply 1	10Mbps Power supply current (all inputs with 5MHz rectangular wave , all outputs with CL=15pF)			-	4.2	5.2	mA
	V <sub>DD2</sub>	Power Supply 2				-	6.5	7.5	
CYP5841Bx, Ex	V <sub>DD1</sub>	Power Supply 1		100Mbps Power supply current (all inputs with 50MHz rectangular wave , all outputs with CL=15pF)		-	4.6	5.5	mA
	V <sub>DD2</sub>	Power Supply 2				-	5.8	6.7	
CYP5842Bx, Ex	V <sub>DD1</sub>	Power Supply 1			100Mbps Power supply current (all inputs with 50MHz rectangular wave , all outputs with CL=15pF)	-	5.0	5.8	mA
	V <sub>DD2</sub>	Power Supply 2				-	5.0	5.8	
CYP5840/5Bx, Ex	V <sub>DD1</sub>	Power Supply 1	100Mbps Power supply current (all inputs with 50MHz rectangular wave , all outputs with CL=15pF)			-	5.2	6	mA
	V <sub>DD2</sub>	Power Supply 2				-	40	45	
CYP5841Bx, Ex	V <sub>DD1</sub>	Power Supply 1		100Mbps Power supply current (all inputs with 50MHz rectangular wave , all outputs with CL=15pF)		-	15	19.8	mA
	V <sub>DD2</sub>	Power Supply 2				-	32	34.7	
CYP5842Bx, Ex	V <sub>DD1</sub>	Power Supply 1			100Mbps Power supply current (all inputs with 50MHz rectangular wave , all outputs with CL=15pF)	-	19	22.8	mA
	V <sub>DD2</sub>	Power Supply 2				-	19	22.8	



## CYP584X

VDD=3.3V 10%, Tamb= 40~125°C

Part No	Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit		
CYP5840/5Bx, Ex	V <sub>DD1</sub>	Power Supply 1	1Mbps Power supply current (all inputs with 500 kHz rectangular wave , all outputs with CL=15pF)	-	4.2	5.5	mA		
	V <sub>DD2</sub>	Power Supply 2		-	2.2	4.1			
CYP5841Bx, Ex	V <sub>DD1</sub>	Power Supply 1		10Mbps Power supply current (all inputs with 5MHz rectangular wave , all outputs with CL=15pF)	-	3.5	4.9	mA	
	V <sub>DD2</sub>	Power Supply 2			-	3.0	4.4		
CYP5842Bx, Ex	V <sub>DD1</sub>	Power Supply 1			100Mbps Power supply current (all inputs with 50MHz rectangular wave , all outputs with CL=15pF)	-	3.5	4.8	mA
	V <sub>DD2</sub>	Power Supply 2				-	3.5	4.8	
CYP5840/5Bx, Ex	V <sub>DD1</sub>	Power Supply 1	100Mbps Power supply current (all inputs with 50MHz rectangular wave , all outputs with CL=15pF)			-	4.2	5.5	mA
	V <sub>DD2</sub>	Power Supply 2				-	4.4	5.7	
CYP5841Bx, Ex	V <sub>DD1</sub>	Power Supply 1		100Mbps Power supply current (all inputs with 50MHz rectangular wave , all outputs with CL=15pF)		-	4.2	5.5	mA
	V <sub>DD2</sub>	Power Supply 2				-	4.7	6.0	
CYP5842Bx, Ex	V <sub>DD1</sub>	Power Supply 1			100Mbps Power supply current (all inputs with 50MHz rectangular wave , all outputs with CL=15pF)	-	4.5	5.5	mA
	V <sub>DD2</sub>	Power Supply 2				-	4.5	5.5	
CYP5840/5Bx, Ex	V <sub>DD1</sub>	Power Supply 1	100Mbps Power supply current (all inputs with 50MHz rectangular wave , all outputs with CL=15pF)			-	5.2	6.0	mA
	V <sub>DD2</sub>	Power Supply 2				--	25.6	28.9	
CYP5841Bx, Ex	V <sub>DD1</sub>	Power Supply 1		100Mbps Power supply current (all inputs with 50MHz rectangular wave , all outputs with CL=15pF)		-	11	13.5	mA
	V <sub>DD2</sub>	Power Supply 2				-	21.7	24.8	
CYP5842Bx, Ex	V <sub>DD1</sub>	Power Supply 1			100Mbps Power supply current (all inputs with 50MHz rectangular wave , all outputs with CL=15pF)	-	14	16.8	mA
	V <sub>DD2</sub>	Power Supply 2				-	14	16.8	

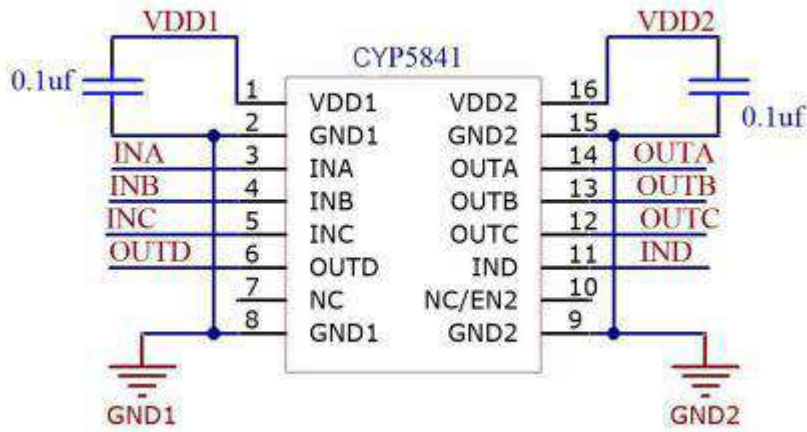


## CYP584X

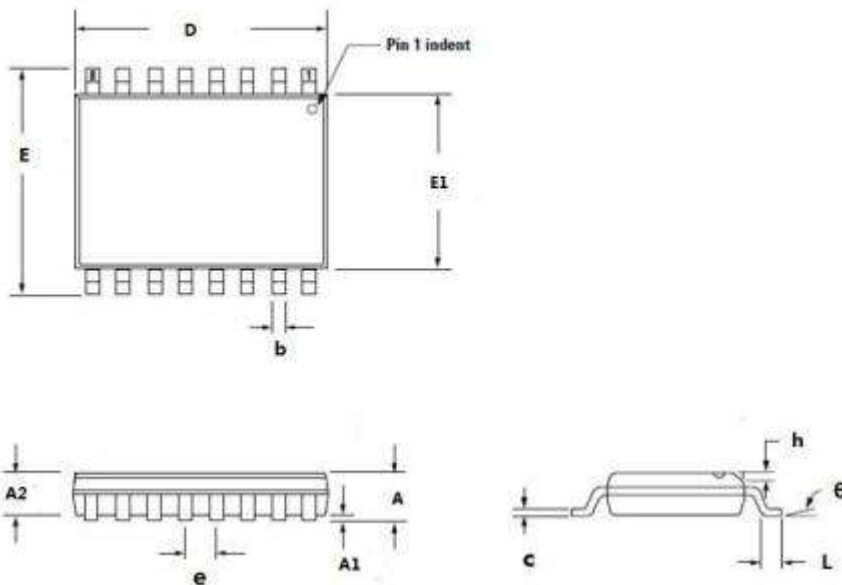
VDD=2.5V 5%, Tamb= 40~125°C

Part No	Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit		
CYP5840/5Bx, Ex	V <sub>DD1</sub>	Power Supply 1	1Mbps Power supply current (all inputs with 500 kHz rectangular wave , all outputs with CL=15pF)	-	4.2	5.5	mA		
	V <sub>DD2</sub>	Power Supply 2		-	2.2	4.1			
CYP5841Bx, Ex	V <sub>DD1</sub>	Power Supply 1		10Mbps Power supply current (all inputs with 5MHz rectangular wave , all outputs with CL=15pF)	-	3.5	4.9	mA	
	V <sub>DD2</sub>	Power Supply 2			-	2.9	4.2		
CYP5842Bx, Ex	V <sub>DD1</sub>	Power Supply 1			100Mbps Power supply current (all inputs with 50MHz rectangular wave , all outputs with CL=15pF)	-	3.3	4.8	mA
	V <sub>DD2</sub>	Power Supply 2				-	3.3	4.8	
CYP5840/5Bx, Ex	V <sub>DD1</sub>	Power Supply 1	10Mbps Power supply current (all inputs with 5MHz rectangular wave , all outputs with CL=15pF)			-	4.2	5.5	mA
	V <sub>DD2</sub>	Power Supply 2				-	3.8	5.1	
CYP5841Bx, Ex	V <sub>DD1</sub>	Power Supply 1		100Mbps Power supply current (all inputs with 50MHz rectangular wave , all outputs with CL=15pF)		-	4.0	5.2	mA
	V <sub>DD2</sub>	Power Supply 2				-	4.2	5.4	
CYP5842Bx, Ex	V <sub>DD1</sub>	Power Supply 1			100Mbps Power supply current (all inputs with 50MHz rectangular wave , all outputs with CL=15pF)	-	4.2	5.3	mA
	V <sub>DD2</sub>	Power Supply 2				-	4.2	5.3	
CYP5840/5Bx, Ex	V <sub>DD1</sub>	Power Supply 1	100Mbps Power supply current (all inputs with 50MHz rectangular wave , all outputs with CL=15pF)			-	5.3	6.2	mA
	V <sub>DD2</sub>	Power Supply 2				--	20	25	
CYP5841Bx, Ex	V <sub>DD1</sub>	Power Supply 1		100Mbps Power supply current (all inputs with 50MHz rectangular wave , all outputs with CL=15pF)		-	9.2	11.0	mA
	V <sub>DD2</sub>	Power Supply 2				-	17	18.1	
CYP5842Bx, Ex	V <sub>DD1</sub>	Power Supply 1			100Mbps Power supply current (all inputs with 50MHz rectangular wave , all outputs with CL=15pF)	-	11.3	13.2	mA
	V <sub>DD2</sub>	Power Supply 2				-	11.3	13.2	

### Application Circuits



### Package Information (SOIC-16)





## CYP584X

Symbol	Min. (mm)	Max. (mm)
A	-	2.65
A1	0.10	0.3
A2	2.05	-
b	0.31	0.51
e	0.20	0.33
D	10.30 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
$\theta$	0°	8°

Note:10.All sizes are in millimeters unless otherwise noted.  
11.Dimensions and tolerances according to ANSI Y14.5M-1994.