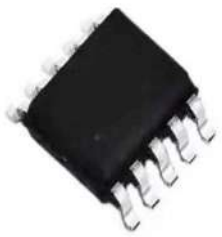
CY Wireless Technology Limited

Built-in Clock, Calibration Free, Single Phase Energy Meter IC with Integrated Oscillator

CYP1842 Datasheet



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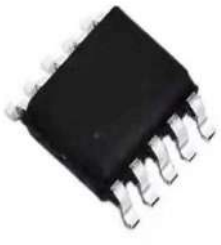
Catalog

1. General Description

CYP1842 is a built-in clock calibration-free energy metering IC, which is suitable for single-phase multi-function electricity meters, smart sockets, smart home appliances and other applications, with more cost-efficient solution.



CYP1842 integrates 2 high-precision Sigma-Delta ADC to measure current and voltage simultaneously. Reference voltage, power management and other analog circuit modules, and processing active power, current and voltage RMS electrical parameters digital signal processing circuit.

CYP1842 can measure electric parameters such as current and voltage RMS, active power, active energy, fast current RMS (for over-current protection), and waveform output and so on. CYP1842 output data through the UART/SPI interface. It is available for the smart socket, smart appliances, single-phase multi-function power meter and information requirement of data acquisition in electricity applications.

CYP1842 has a patented anti-creep design, which can be combined with reasonable external hardware design to ensure that the noise energy cannot be calculated in the energy pulse when there is no load.

2. Features

- Two independent Sigma-Delta ADC, one current and one voltage
- Current RMS range (10mA ~ 30A) @1mOhm
- The range of Active energy (1w ~ 6600w) @1mohm@220V
- Measure current, voltage RMS, fast current RMS, active power
- The batch factory gain error is less than 1%, and the peripheral components can be free of calibration under certain conditions
- The current channel support over-current monitoring function, the threshold and response time can be configured
- Voltage/current zero-crossing logic output
- Built-in waveform register，provide sampled waveform data for load type analysis
- SPI (maximum speed 900kHz)/ UART (4800 ~38400bps) communication
- On-chip power supply monitoring, IC reset when VDD is lower than 2.7V(typical)
- On-chip reference 1.218v(typical)
- On-chip 4MHz oscillator circuit
- Single 3.3V supply, low power consumption 10mW (typical)
- Package：SSOP10L

3. Order specification

Part No	Package	Manner of Packing	Devices per bag/reel
CYP1842	SSOP10L	Reel	2500PCS

4. Block Diagram

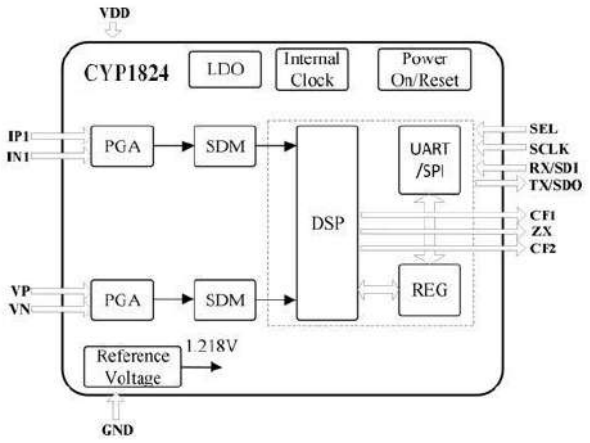


Figure 1 Internal block diagram

5. Pin Assignment

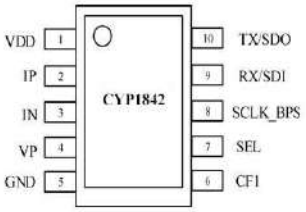


Figure 2 SSOP10L

TSSOP14L	SSOP10L	Pin Name	Description
1	1	VDD	Power supply (3.3V)
2,3	2,3	IP,IN	Analog input for Current Channel, this differential voltage input has a maximum input range of ±42mVp-p (30mV RMS)
4	4	VP	Analog input for Voltage Channel, this voltage input has a maximum input range of ±100mVp-p (70mV RMS)
5	5	GND	Ground reference
6		A1	Chip Address set for UART interface.Internal default pull-down.

7		A2_NCS	Chip select for SPI interface. Chip Address set for UART interface.Internal default pull-down.
8		CF2	Logic output. See the OT_FunX register configuration section
9		ZX	Zero crossing Voltage logic output.See the OT_FunX register configuration section
10	6	CF1	Logic output. See the OT_FunX register configuration section
11	7	SEL	UART/SPI mode selection (0:UART 1:SPI), internal pull-down resistance, disconnect is 0 level (UART), connected directly to VDD is high level (SPI)
12	8	SCLK_BPS	Serial Clock input for SPI. If using UART, this pin is used to config baud rate of UART
13	9	RX/SDI	UART/SPI multiplex pin，UART RX/SPI DIN
14	10	TX/SDO	UART/SPI multiplex pin, UART TX/SPI DOUT, need external pull-up resistor for UART interface.

6. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power Voltage VDD	VDD	-0.3～+4	V
Analog Input Voltage to GND	IP1,VP	-4～+4	V
Digital Input Voltage to GND	UART_SEL,RX/SDI	-0.3～VDD+0.3	V
Digital Output Voltage to GND	CF,TX/SDO	-0.3～VDD+0.3	V
Operating Temperature Range	T	-40～+85	℃
Storage Temperature Range	Tstg	-40～+85	℃

Note: Unless specified otherwise, Tamb= 25℃

7. Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply	VDD		3.0		3.6	V
Power Dissipation	Iop	VDD=3.3V		3		mA
Measuring range		4000:1 Input dynamic range				
Active energy measurement accuracy (large signal)		30A~100mA Input@ 1mohm sampling resistor		0.2		%
Active energy measurement accuracy (small signal)		100mA~50mA Input@ 1mohm sampling resistor		0.4		%
Active energy measurement accuracy (tiny signal)		50mA~10mA Input@ 1mohm sampling resistor		0.6		%
RMS measurement accuracy(large signal)		30A~100mA Input@ 1mohm sampling resistor		0.2		%
RMS measurement accuracy(small signal)		100mA~50mA Input@ 1mohm sampling resistor		2		%
RMS measurement		50mA~10mA Input@		6		%

accuracy(tiny signal)		1mohm sampling resistor				
Fast RMS response time	50Hz	Can be set to cycle/half cycle	10		160	mS
	60Hz		8.3		133	mS
Zero-crossing signal output delay				570		uS
Measurement error caused by phase angle between channels (capacitance)	PF08err	Phase advance 37 ° (PF=0.8)			0.5	%
Measurement error caused by phase angle between channels (sensibility)	PF05err	Phase delay 60 ° (PF=0.5)			0.5	%
AC power suppression (output frequency amplitude variation)	ACPSRR	IP/N=100mV			0.1	%
DC power suppression (output frequency amplitude variation)	DCPSRR	VP/N=100mV			0.1	%
Analog input level (current)		Differential current input (peak)			42	mV
Analog input level (voltage)		Differential voltage input (peak)			100	mV
Analog input impedance				370		kΩ
SEL pull-down resistor		SEL(pull-down)		56.9		kΩ
Analog input bandwidth		(-3dB)		3.5		kHz
Internal voltage reference	Vref			1.218		V
Logic input high-level		VDD=3.3V±5%	2.6			V
Logic input low-level		VDD=3.3V±5%			0.8	V
Logic output high-level		VDD=3.3V±5% IOH=5mA	VDD -0.5			V
Logic output low-level		VDD=3.3V±5% IOL=5mA			0.5	V

Note：Unless specified otherwise, Tamb= 25℃

All voltage values take GND terminal potential as reference point.

Test conditions VDD=3.3V, Built-in crystal oscillator, electric energy is measured by CF output.

8. Internal Register Description

8.1 Register list

Address	Symbol	External R/W	Internal R/W	Bits	Default	Description
Electrical parameter register (read only)						
0x01	I_WAVE	R	W	20	0x00000	Current waveform register, signed
0x02	V_WAVE	R	W	20	0x00000	Voltage waveform register, signed
0x03	I_RMS	R	W	24	0x000000	Current RMS, unsigned
0x04	V_RMS	R	W	24	0x000000	Voltage RMS register, unsigned
0x05	I_FAST_RMS	R	W	24	0x000000	Current fast RMS, unsigned
0x06	WATT	R	W	24	0x000000	Active power register, signed
0x07	CF_CNT	R	W	24	0x000000	Active energy pulse count, unsigned
0x08	FREQ	R	W	16	0x4E20	Line voltage frequency
0x09	STATUS	R	W	10	0x000	System Status
User operated register (read and write)						
0x12	I_RMSOS	R/W	R	8	0x00	Current RMS Offset
0x14	WA_CREEP	R/W	R	8	0x0B	Active power No-load threshold
0x15	I_FAST_RMS_TH	R/W	R	16	0xFFFF	Current fast RMS threshold
0x16	I_FAST_RMS_CYC	R/W	R	3	0x1	Line cycle for Current fast RMS measurement
0x17	FREQ_CYC	R/W	R	2	0x3	Line cycle for Line voltage frequency measurement
0x18	OT_FUNX	R/W	R	6	0x24	Logic output configuration
0x19	MODE	R/W	R	10	0x87	User mode selection
0x1A	GAIN_CR	R/W	R	2	0x2	Current channel gain
0x1C	SOFT_RESET	R/W	R	24	0x000000	Software reset, CYP1842 resets if 0x5a5a5a is written to this register
0x1D	USR_WRPROT	R/W	R	8	0x00	User write protection. Only 0x55 is written to this register, the user operation register can be written

Note: the data frame of communication protocol is 24bit, and the upper invalid bit need be supplemented with 0.

8.2 Special Register Description

8.2.1 User mode selection register（Note: X indicates either 0 or 1）

0x18	MODE	User mode selection register		
No.	name	default value	description	
[1:0]	Reserved	b11	reserved	
[2]	CF_EN	b1	Active energy and pulse output Enable	0：Disable
				1：Enable

[3]	RMS_UPDATE_SEL	b0	Selection of refresh time for RMS	0：400ms 1：800ms
[4]	Reserved	b00	reserved	
[5]	AC_FREQ_SEL	b0	Selection of AC frequency	0：50Hz 1：60Hz
[6]	CF_CNT_CLR_SEL	b0	Clear after read of CF_CNT register Enable	0：Disable 1：Enable
[7]	CF_CNT_ADD_SEL	b1	Mode selection of active energy pulse accumulation	0：Signed accumulation mode 1: Absolute accumulation mode
[9:8]	UART_RATE_SEL	b00	UART communication Baud rate selection	0x：The baud rate is decided by the external pin SCLK_BPS SCLK_BPS=0, 4800bps SCLK_BPS=1, 9600bps 10：19200bs 11：38400bps
[23:10]	Reserved	b0	reserved	

8.2.2 Logic Output configuration register

0x18	OT_FUNX	Logic Output configuration register	
No.	**name**	**default value**	**description**
[1:0]	CF1_FUNX_SEL	b00	CF1 output selection bit: 00：Active energy calibration pulse Output 01：Logic output of over-current event 10：Logic output of zero crossing voltage 11： Logic output of zero crossing current
[3:2]	CF2_FUNX_SEL	b01	CF2 output selection bit: 00：Active energy calibration pulse Output 01：Logic output of over-current event 10：Logic output of zero crossing voltage 11：Logic output of zero crossing current
[5:4]	ZX_FUNX_SEL	b10	ZX output selection bit: 00：Active energy calibration pulse Output 01：Logic output of over-current event 10：Logic output of zero crossing voltage 11：Logic output of zero crossing current
[23:6]	Reserved	b0	reserved

8.2.3 System Status register

0x1B	STATUS	System Status register	
No.	**name**	**default value**	**description**
[0]	CF_REVP_F	b0	Pulse CF energy is indicated in reverse, negative energy is set to 1
[1]	CREEP_F	b0	When the active power is less than the active anti-creep value, set it to 1
[7:2]	Reserved	b0	reserved

[8]	I_ZX_LTH_F	b0	Indication of current zero crossing output stutas
[9]	V_ZX_LTH_F	b0	Indication of voltage zero crossing output stutas
[23:10]	Reserved	b0	reserved

9. Theory of Operation

CYP1842 is mainly divided into analog signal processing and digital signal processing. The analog part mainly includes two-channel PGA, two-channel Sigma-Delta ADC, internal clock, Power-on and power-off monitoring(Power on/reset), LDO and other related simulation modules， The digital part is digital signal processing module(DSP).

9.1 Current and voltage transient waveform measurement

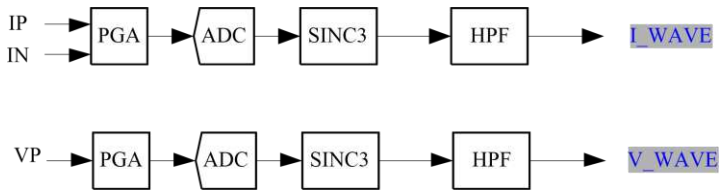


Figure 3

As the picture above shows, the current and voltage get two way of 1bit PDM for digital module through analog module amplifier (PGA) and high-precision analog-to-digital converter (ADC), Digital module through down-sampling filter (SINC3), high-pass filter (HPF) and channel bias correction and such as module，obtain the required current waveform data and voltage waveform data (I_WAVE，V_WAVE).

The current and voltage waveform data are updated at a rate of 7.8Kbps. Each sampling data is 20bit signed and stored in the waveform data register (I_WAVE, V_WAVE).The SPI rate configuration is greater than 375Kbps, and the waveform value of one channel can be read continuously.

Address	Symbol	External	Internal	Bits	Default	Description
		R/W	R/W			
0x01	I_WAVE	R	W	20	0x00000	Current waveform register
0x02	V_WAVE	R	W	20	0x00000	Voltage waveform register

9.2 Active Power

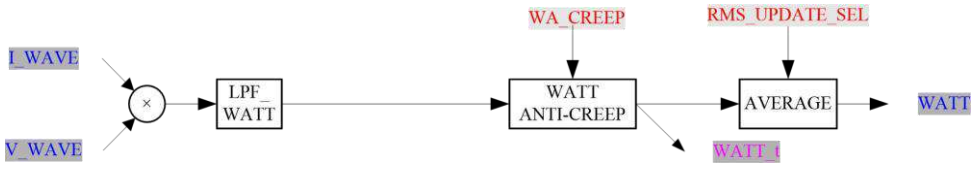


Figure 4

Address	Symbol	External	Internal	Bits	Default	Description
		R/W	R/W			

0x06	A_WATT	R	W	24	0x000000	Active power register, signed

Formula for calculating active power: $WATT = \frac{3537 * (\ ) * \cos(\varphi)}{r^2}$

I(A) and V(V) are the voltage RMS of analog input PIN(IP&IN, VP&GND), φ is the phase angle between I(A) and V(V) (AC signal), Vref is the on-chip reference voltage, the typical value is 1.218V.

This register indicates whether the active power is positive or negative. Bit[23] is the symbol Bit. Bit[23]=0 means the current power is positive and Bit[23]=1 means the current power is negative, in complement form.

9.3 Active power anti-creep

CYP1842 has the patented power anti-creep function, which ensures that the power of board level noise will not accumulate when there is no load.

This active power no-load threshold register(WA_CREEP) is 8bit unsigned data, default value is 0BH. The corresponding relationship between this value and the active power register value is shown in the following formula. When the absolute value of the input active power signal is less than this value, the output active power is set to 0. This can make the value of the active power register is 0 and the energy does not accumulate in the case of no load, even if there is a tiny noise signal.

Address	Symbol	External	Internal	Bits	Default	Description
		R/W	R/W			
0x14	WA_CREEP	R/W	R	8	0x0B	Active power no-load threshold register

Set WA_CREEP based on the value of the power register WATT, their corresponding relationship as below:

$WA\_CREEP = * \frac{256}{3125}$

When the channel is in the anti-creep state, the RMS current register of this channel is also set to 0.

9.4 Energy Measurement

CYP1842 provides energy pulse measurement. The active instantaneous power is integrated by time to get active energy and output calibration pulse CF in proportion. CFA_CNT register saves the count of output energy pulse.

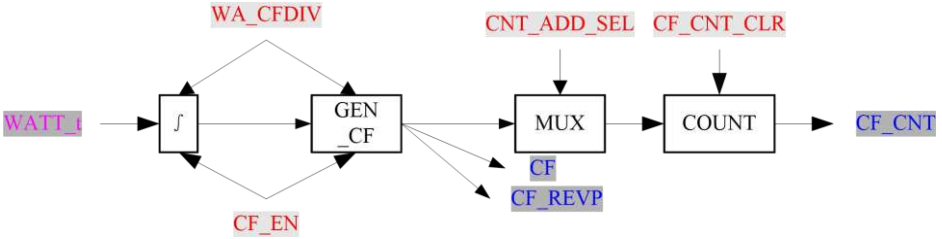


Figure 6

Address	Symbol	External	Internal	Bits	Default	Description
		R/W	R/W			

0x07	CF_CNT	R	W	24	0x000000	Active energy pulse count，unsigned

CYP1842 provide active energy via CF_CNT register. The number of pulses can also be counted directly from CF1/CF2/ZX pins by I/O interrupt after configuring the OT_FUNX register.When the active energy pulse period is shorter than 160mS, the duty cycle of the pulse output is 50%, when the pulse period is longer than 160mS, the high-level fixed pulse width is 80mS.

0x19	**MODE**	**Operating mode register**		
No.	**name**	**default value**	**description**	
[2]	CF_EN	0b1	Active energy and pulse output Enable	0：Disable
				1：Enable
[6]	CF_CNT_CLR_SEL	0b0	Clear after read of CF_CNT register Enable	0：Disable
				1：Enable
[7]	CF_CNT_ADD_SEL	0b1	Mode selection of active energy pulse accumulation	0：Signed accumulation mode
				1：Absolute accumulation mode

CF_EN is the main switch of energy pulse output.After shutdown, CF_CNT stops counting and CF1/CF2/ZX pins stop output power pulse counting.

The CF_CNT_CLR_SEL register can be used to determine whether the CF count register (CF_CNT) is cleared after reading.The pulse energy accumulation mode can be selected by CF_CNT_ADD_SEL.

Note: the CF_CNT register is the accumulation mode of absolute value of electric energy pulse.

Cumulative time of each CF pulse $t_{CF}=\frac{1638.4*256}{WATT}$

Where: WATT is the value of active power register（WATT）。

9.5 Current and Voltage RMS

The RMS of these channels is shown in the figure below. After the square circuit (X^2), the low-pass filter (LPF_RMS) and the ROOT circuit (ROOT), the instantaneous value RMS_t of RMS is calculated, and then the average value of the two channels (I_RMS, V_RMS) is calculated.

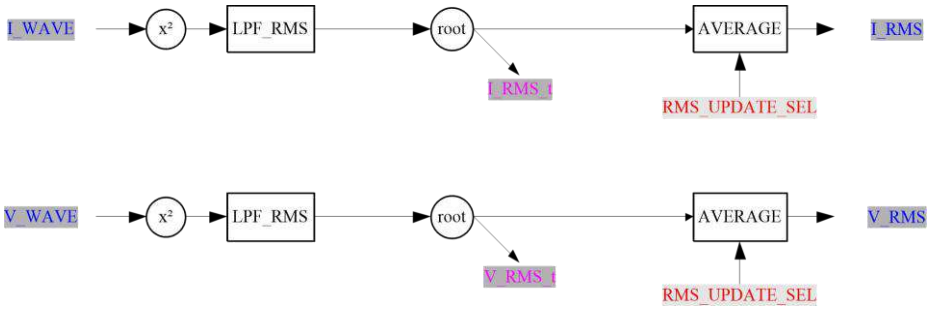


Figure 6

Address	Symbol	External	Internal	Bits	Default	Description
		R/W	R/W			
0x03	I_RMS	R	W	24	0x000000	Current RMS register, unsigned
0x04	V_RMS	R	W	24	0x000000	Voltage RMS register, unsigned

0x19	MODE	User mode selection register		
No.	name	default value	description	
[3]	RMS_UPDATE_SEL	0b0	RMS register update rate	0：400ms
				1：800ms

Set MODE[3].RMS_UPDAT_SEL, the average refresh time of RMS can be selected as 400ms or 800ms, and the default value is 400ms. When a current channel is in anti-creep state, the RMS of the current channel is 0.

The current RMS conversion formula: $I\_RMS = \frac{305978*()}{r}$

The voltage RMS conversion formula: $V\_RMS = \frac{73989*()}{r}$

Vref is the reference voltage, the typical value is 1.218V.

I(A) is the input signal between IP1 and IN1 pins (mV), and V(V) is the input signal of VP pins (mV).

9.6 Over-current Detection

CYP1842 can quickly collect effective current value to realize over-current detection function.The absolute value of I_WAVE_F is accumulated in half cycle or cycle time and stored in I_FAST_RMS register.Compared with the current fast RMS threshold register I_FAST_RMS_TH, the output over-current is interrupted by the pin.

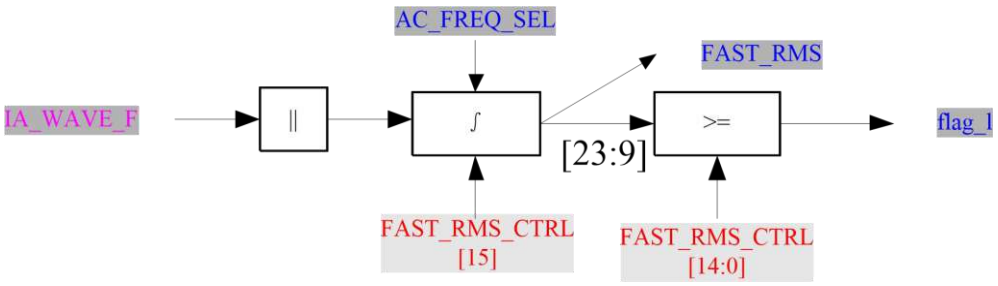


Figure 7

Address	Symbol	External	Internal	Bits	Default	Description
		R/W	R/W			
0x15	I_FAST_RMS_TH	R/W	R	16	0xFFFF	Current fast RMS threshold

Set the fast RMS threshold (over-current threshold) using the I_FAST_RMS_TH fast RMS threshold register.

Address	Symbol	External	Internal	Bits	Default	Description
		R/W	R/W			
0x05	I_FAST_RMS	R	W	24	0x000000	Current fast RMS, unsigned

Compare the Bit[23:8] of I_FAST_RMS register with the over-current threshold I_FAST_RMS_TH [15:0]. If it is greater than or equal to the set threshold, the over-current alarm output indicates the high level output of pin CF1/CF2/ZX.CF1/CF2/ZX is set by the OT_FUNX output configuration register.

Address	Symbol	External	Internal	Bits	Default	Description	
		R/W	R/W				
0x16	I_FAST_RMS_CYC	R/W	R	3	0x1	Line cycle for Current fast RMS measurement	
						000	0.5 cycles
						001	1 cycle
						010	2 cycles
						011	4 cycles
						other	8 cycles

Set the fast RMS refresh cycle through I_FAST_RMS_CYC line cycle for Current fast RMS measurement register. Cycle wave can be set to 50H or 60Hz according to MODE[5]. If select 50Hz, refresh 1 cycle (every 20ms) by default.If the fastest 0.5 cycle accumulation is selected, the error of the I_FAST_RMS register will be relatively large.

$$I\_FAST\_RMS \approx I\_RMS * 0.363$$

It is important to note that the algorithm for fast RMS is different from that for RMS. Fast RMS is only used for measurement judgment when the signal is large. Fast RMS measurements at small signals are inaccurate due to the inclusion of dc bias components.

0x19	MODE	Operating mode register		
No.	name	default value	description	
[5]	AC_FREQ_SEL	0b0	AC frequency selection	0：50Hz
				1：60Hz

MODE [5] is used to config AC frequency.

9.7 Line Voltage Frequency Detection

CYP1842 provides a frequency measurement of the voltage channel. Refresh every set cycle (FREQ_CYC), the detection is the full wave voltage waveform.

Address	Symbol	External	Internal	Bits	Default	Description	
		R/W	R/W				
0x08	FREQ	R	W	16	0x4e20	Line voltage register, unsigned	
0x17	FREQ_CYC	R/W	R	2	0x3	Line voltage refresh time setting register	
						00	2 cycles
						01	4 cycles
						10	8 cycles
						11	16 cycles

The frequency measurement has a resolution of 2us/LSB(500KHz CLOCK)， which represents 0.01% when the line frequency is 50Hz and 0.012% when the line frequency is 60Hz.Line voltage register (FREQ) and the actual line voltage frequency conversion relationship：

$$\text{measure} = \frac{2*}{RR}$$

In the default mode f_s=500KHz ； For the 50Hz electric city Network, the measured FREQ value is 20000(decimal), and for the 60Hz electric city Network, the measured FREQ value is 16667(decimal).

In addition, when the RMS voltage is lower than the zero-crossing threshold, the line voltage frequency detection is disable.

9.8 Zero Crossing Detection

CYP1842includes a zero-crossing detection on voltage and current channel. Zero crossing signal can be output by pin CF1/CF2/ZX, pin output zero means positive half cycle of waveform, pin output 1 means negative half cycle of waveform. The delay relative to the actual input signal is 570us.

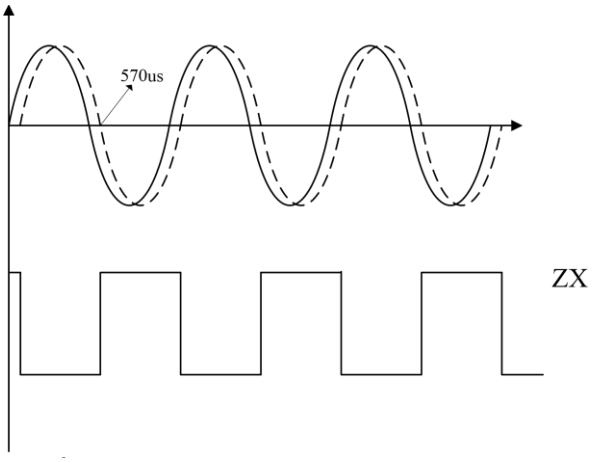


Figure 8

0x18	OT_ FUNX	Output configuration register	
No.	**name**	**default value**	**description**
[1:0]	CF1_FUNX_SEL	0b00	CF1 output selection bit: b00:Active energy calibration pulse Output b01:Logic output of over-current event b10:Logic output of zero crossing voltage b11:Logic output of zero crossing current
[3:2]	CF2_FUNX_SEL	0b01	CF2 output selection bit: b00:Active energy calibration pulse Output b01:Logic output of over-current event b10:Logic output of zero crossing voltage b11:Logic output of zero crossing current
[5:4]	ZX_FUNX_SEL	0b10	ZX output selection bit: b00:Active energy calibration pulse Output b01:Logic output of over-current event b10:Logic output of zero crossing voltage b11:Logic output of zero crossing current

The output pin is configured by OT_ FUNX (SSOP10L package only CF1).

0x19	STATUS	Working status register		
No.	**name**	**default value**	**description**	
[8]	I_ZX_LTH_F	0b0	indication of current zero crossing output stutas	0：current zero crossing higher than threshold 1：current zero crossing below threshold
[9]	V_ZX_LTH_F	0b0	indication of voltage	0：voltage zero crossing

			zero crossing output stutas	higher than threshold
				1：voltage zero crossing below threshold

If the RMS of voltage or current is too low, the output signal of zero crossing detection is unstable.

The fixed threshold of current channel is approximately set to a range of 64:1 of the input full scale. The fixed threshold of voltage channel is approximately set to a range of 32:1 of the input full scale. If any input signal falls below these levels, no zero-crossing signals are produced by CYP1842, the ZX logic output keep low level.

10. Communication Interface

CYP1842 provides SPI/UART communication interfaces, these communication interface use the same group of pins. So only one method of communication can be used in each design. Register data are sent as 3 bytes (24bit). The data is fixed 3 bytes, if valid data bytes are less than 3 bytes, invalid bits are filled with 0.

10.1 SPI

- If SEL Pin is pulled up to VDD, the communication method is SPI
- Slave mode
- Half-duplex communication, the communication rate can be configured, the maximum communication rate is 900khz
- 8-bit data transmission, MSB first, LSB last
- Clock polarity / phase (CPOL = 0, CPHA = 1)
- Three or four wire communication method.In three wire mode, A2_NCS is connected to GND.When A2_NCS is controlled by MCU, it is equivalent to four-wire communication.

10.1.1 Operation Mode

The master device works in Mode1：CPOL=0，CPHA=1，In idle state, SCLK is at low-level. Data is transmitted on the first edge, which is the transition from low level to high level of SCLK, so data is received on the falling edge and data is sent on the rising edge.

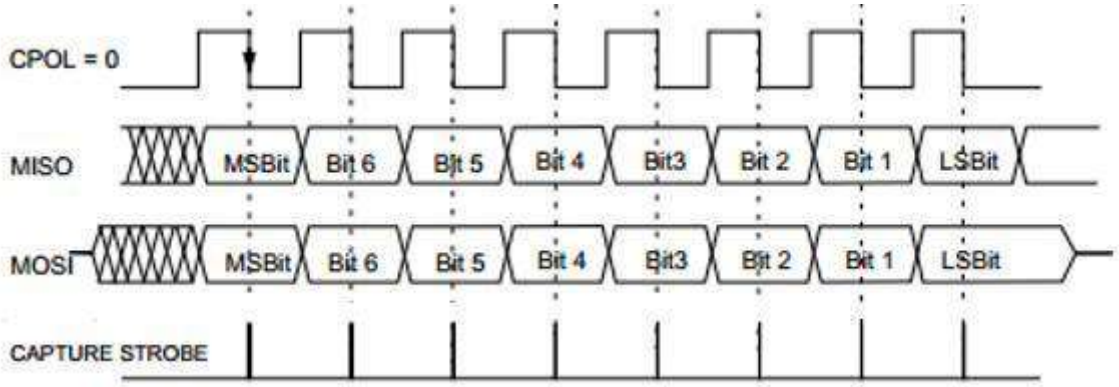


Figure 9

10.1.2 Frame Structure

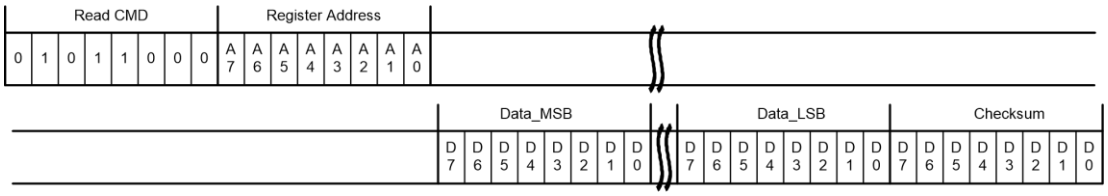
In SPI communication method, first send 8bit initial byte (0x58) or (0xA8), (0x58) is read operation identification byte, (0xA8) is write operation identification byte,and then send the register address byte,determine to access the address of a register (See register list of CYP1842) .The following figure shows the order of data transfer for read and write operations respectively. After one frame transmission, CYP1842 re-enters communication mode. A complete read/write operation contain 48 cycles.

There are two frame structures, which are described as follows：

1）Write operation frame

where the CHECKSUM byte =((0xA8 + ADDR + DATA_H + DATA_M+ DATA_L) & 0xFF) and then inverted by bit.

2）Read operation frame



where the CHECKSUM byte =((0x58 + ADDR + DATA_H + DATA_M+ DATA_L) & 0xFF) and then inverted by bit.

Note: the register data is fixed to 3 bytes (The high byte comes first, the low byte comes last,if the effective byte of the register data is less than 3 bytes, the invalid bit should be filled with 0).

10.1.3 Write Operation Timing

The serial write timing is performed as follows. The frame identification byte {0xA8} indicates that the data communication operation is data writing.ADDR is the address of the register to which data is to be written， MCU will prepare the data bits that need to be written to CYP1842 before the lower edge of SCLK, where the lower edge of this clock begins to move register data.All remaining bits of register data are also left shifted along the lower edge of the SCLK（Figure 10）

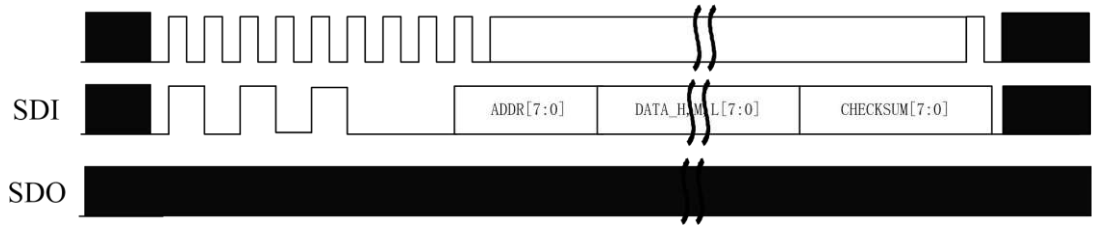


Figure 10

10.1.4 Read Operation Timing

During the data read operation, CYP1842 shifts the corresponding data to the SDO pin on the rising edge of SCLK. SDO keeps unchanged during SCLK =1.MCU can sample SDO value before the next falling edge. MCU must send a read command frame first before read operation.

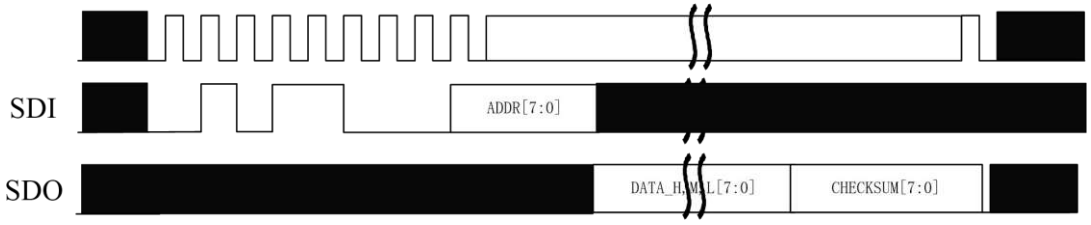


Figure 11

When CYP1842 is in communication mode, the frame identification byte {0x58} indicates that the data communication operation is data reading. After receiving the register address, CYP1842 starts to shift out the data in the register on the rising edge of SCLK (Figure 14). All remaining bits of the register data are shifted out on subsequent rising SCLK edges.Therefore, on the falling edge of SCLK, an external device can sample the output data of the SPI. Once the read operation is completed, SPI re-enters the communication mode. SDO enters a high-impedance state on the falling edge of the last SCLK signal.

10.1.5 Fault-tolerant mechanism of SPI interface

SPI supports soft reset function, reset SPI interface individually by sending 6 bytes of 0xFF.

10.2 UART Communication methods

10.2.1 Summarize

● CYP1842 can adopt UART communication mode. UART interface only needs two low speed photocoupler to achieve isolated communication

● SEL pin connected to GND, SEL = 0, UART communication method

● slave mode

● Half duplex communication, the baud rate can be configured to 4800bps,9600bps, 19200bps,38400bps.

● 8-bit data transmission, no parity bit, stop bit 1

● Support packet reading

● TSSOP14L package can support the chip address function of the device, and the IC Address can be configurated to 0~3 by pins [A2_NCS, A1]. These IC Address set allow communication with multiple devices (maximum 4 pcs of CYP1842) on the one UART interface of MCU

10.2.2 Baud Rate Configuration

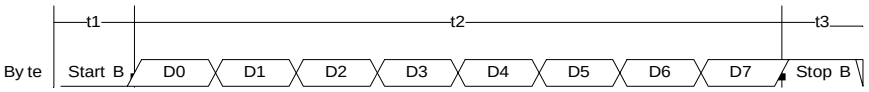
Configurate Baud Rate by register UART_RATE_SEL(MODE[9:8]) and SCLK_BPS pin.

0x19	**MODE**	**Operating mode register**			
No.	**name**	**default value**	**description**		
[9:8]	UART_RATE_SEL	0b00	UART communication Baud rate	00	SCLK_BPS pin=0:4800bps
					SCLK_BPS pin=1:9600bps
				01	Same as 00

			selection	10	19200bps
				11	38400bps

When the chip is powered on each time, the RATE_SEL reset value is 0x0, and the baud rate is determined according to the pin SCLK_BPS.

10.2.3 Per Byte Format



Take baud rate = 4800bps as an example：

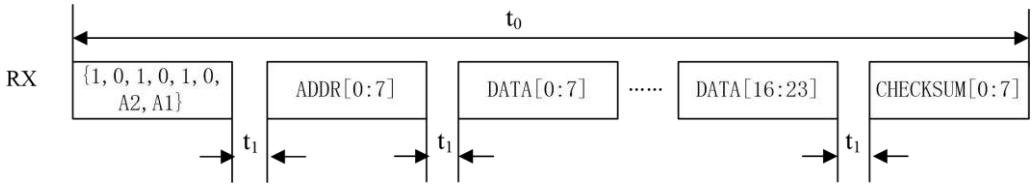
Start bit low level duration t1=208us

Effective data bit duration t2=208*8=1664us

Stop bit high level duration t3=208us

10.2.4 Write Timing

The UART data writing sequence of the host is shown in the figure below. The host first sends command bytes {1,0,1,0,1,0, A2, A1}, and then sends the register address(ADDR) that need to write data. Next, the three data bytes are sent (the low byte is first, the high byte is later, if the valid bytes of the data is less than 3 bytes, the invalid byte is supplemented with 0), and finally the CHECKSUM byte is sent.



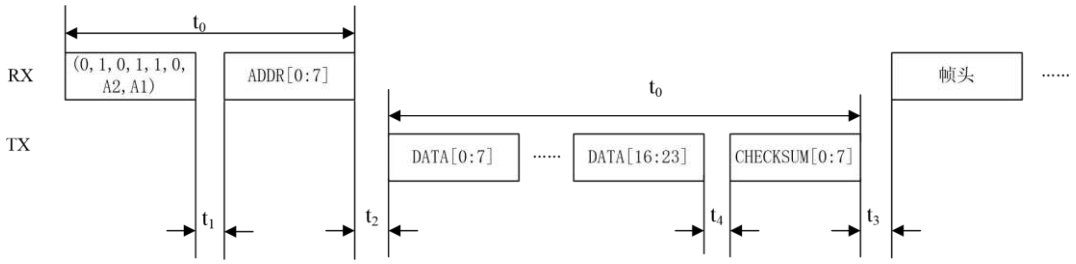
{1,0,1,0,1,0, A2, A1} is the frame initial byte of the write operation.If {A2,A1}=10 ， the CYP1842 address is 2, the frame initial byte is 0XAA.

ADDR is the register address of CYP1842 that need to write data.

The CHECKSUM byte is ({1,0,1,0,1,0,A2,A1}+ADDR+DATA[7:0]+DATA[15:8]+DATA[23:16]) &0xFF then inverted by bit.

10.2.5 Read Timing

The UART data reading sequence of the host is shown in the figure below. The host first sends command byte {0,1,0,1,1,0, A2, A1}, and then sends the register address(ADDR) to be read. Next, CYP1842 will return three data bytes (low byte comes first, high byte comes last, invalid bytes supplemented with 0 if valid byte is less than 3 bytes), and finally CHECKSUM byte.



{0,1,0,1,1,0, A2, A1} is the frame initial byte of read operation, assuming {A2,A1}=10，the CYP1842 address is 2, the frame initial byte is 0x5A，ADDRis the register address of CYP1842 that need to read data.

The CHECKSUM byte is ({0,1,0,1,1,0,A2,A1}+ADDR+DATA[7:0]+DATA[15:8]+DATA[23:16]) & 0xFF then inverted by bit.

Note：the IC Address of SSOP10L package is 0, {A2,A1}=00。

Timing Description：

	Description	Min	Type	Max	Unit
t1	Byte-to Byte Delay by MCU	0		20	mS
t2	Delay between the end of MCU sending register address and CYP1842 sending byte in read operation		150		uS
t3	Frame-to-Frame delay	0.5			uS
t4	Byte-to Byte Delay by CYP1842		0		uS

10.2.6 Packet sending mode

The MCU sends a packet of two bytes "{0,1,0,1,1,0, A2, A1} + 0xAA", CYP1842 will return a full electric parameter data packet. A total of 22 bytes are returned, which takes about 48ms when 4800bps is used.All electric parameter package format:

	Send byte order	content
HEAD	0	0x55
I_RMS	1	I_RMS[7:0]
	2	I_RMS[15:8]
	3	I_RMS[23:16]
V_RMS	4	V_RMS[7:0]
	5	V_RMS[15:8]
	6	V_RMS[23:16]
I_FAST_RMS	7	I_FAST_RMS[7:0]
	8	I_FAST_RMS[15:8]
	9	I_FAST_RMS[23:16]
WATT	10	WATT[7:0]
	11	WATT[15:8]
	12	WATT[23:16]
CF_CNT	13	CF_CNT[7:0]
	14	CF_CNT [15:8]
	15	CF_CNT [23:16]

	Send byte order	content
FREQ	16	FREQ [7:0]
	17	FREQ [15:8]
	18	0x00
STATUS	19	STATUS [7:0]
	20	0x00
	21	0x00
CHECKSUM	22	

checksum=({0,1,0,1,1,0,A2,A1} + 0x55 + data1_l + data1_m + data1_h +…….) & 0xff then inverted by bit.

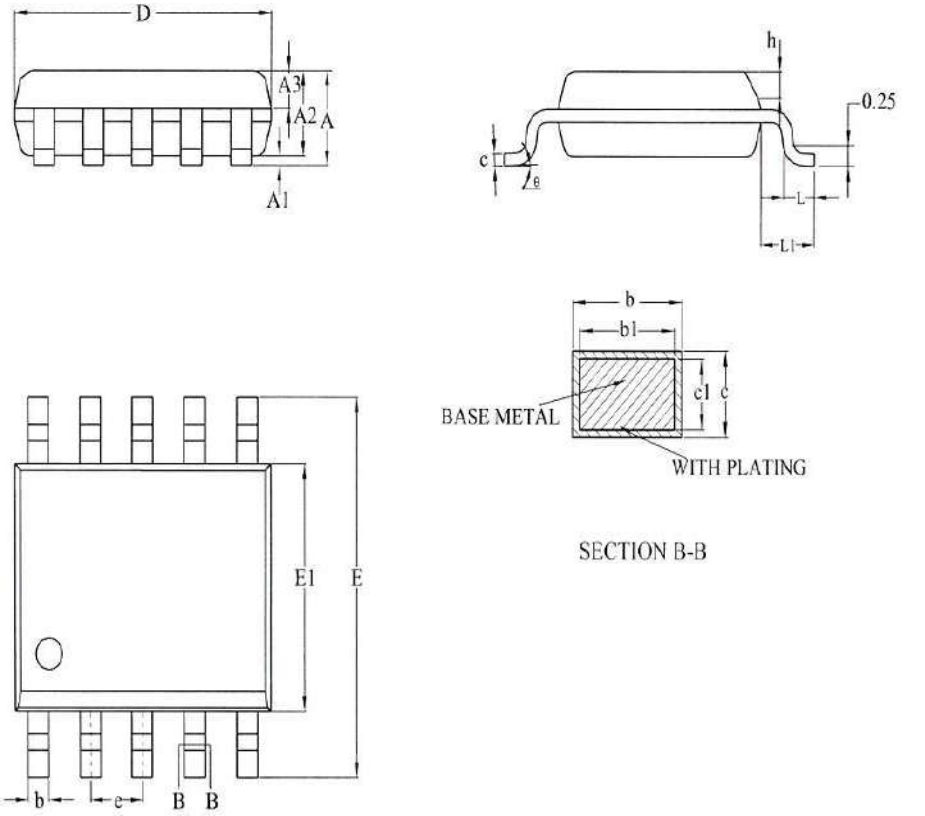
10.2.7 Protection mechanism of UART interface

CYP1842 UART communication provides timeout protection mechanism:

- Frame timeout reset. If Byte-to Byte Delay by master exceeds 20ms, UART interface will reset.
- Manual reset, the UART interface of CYP1842 continuously receives more than 32 "0", and theUART interface is reset.
- Frame identification byte or checksum byte error occurs, then frame data is discarded

Note: In multi-chip communication in UART mode, the next frame can be sent only after a frame timeout time or a manual reset is sent.

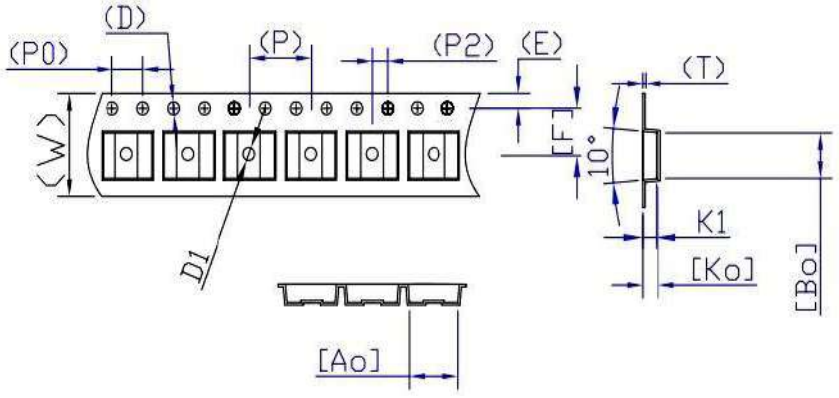
11. Package Information（SSOP10L）



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.00BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Reel size

ITEM	W	A0	B0	D	D1	E	F	K1	K0	P0	P2	P	T
DIM	12.0	6.55	5.40	1.5	1.5	1.75	5.50	1.85	2.0	4.0	2.0	8.0	0.30
TOLE	+0.3 −0.3	±0.10	±0.10	+0.1 −0.0	+0.1 −0.0	±0.1	±0.10	±0.05	±0.10	±0.1	±0.1	±0.1	±0.05



12. Special Instructions

The company reserves the right of final interpretation of this specification.

Version Change Description

Version：V1.03 Author：Lifeng Liu Time：2021.9.09

Modify the record：

1. Re-typesetting the manual and checking some data