General Description

The CY310 is a UHF ASK receiver IC in a SOP-8 package which operates at 300MHz to 450MHz with typical receiving sensitivity of -114dBm.

The CY310 is a Weaver architecture receiver for ASK and OOK modulation such as pulse width modulation, variable pulse modulation, Manchester modulation and so on. The Weaver receiver also provides image rejection function to remove the image band and selects the desired signal.

The high integrated CY310 uses the 8-Lead Small Outline Package (SOP-8), also no extra external component is required except one capacitor (CTH), reference crystal and antenna matching network.

The CY310 additionally provides the Shut Down function pin (SHDN) and CTH pin, the CTH with different external capacitor can satisfy various data profile.

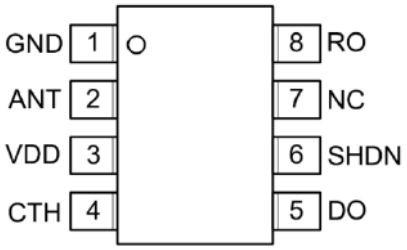
Features

- 300MHz to 450MHz Frequency Range
- -114dBm High Sensitivity, 1kbps and BER 10E-2 @315MHz and 433.92MHz
- Image Rejection Function
- Low Power Consumption
- Excellent Selectivity and Noise Rejection
- No External IF Filter Required
- Low External part count
- SOP-8 Package Type for CY310

Applications

※ Automotive Remote Keyless Entry (RKE)
※ Remote Control System
※ Access Control System
※ Home Automation
※ Toys

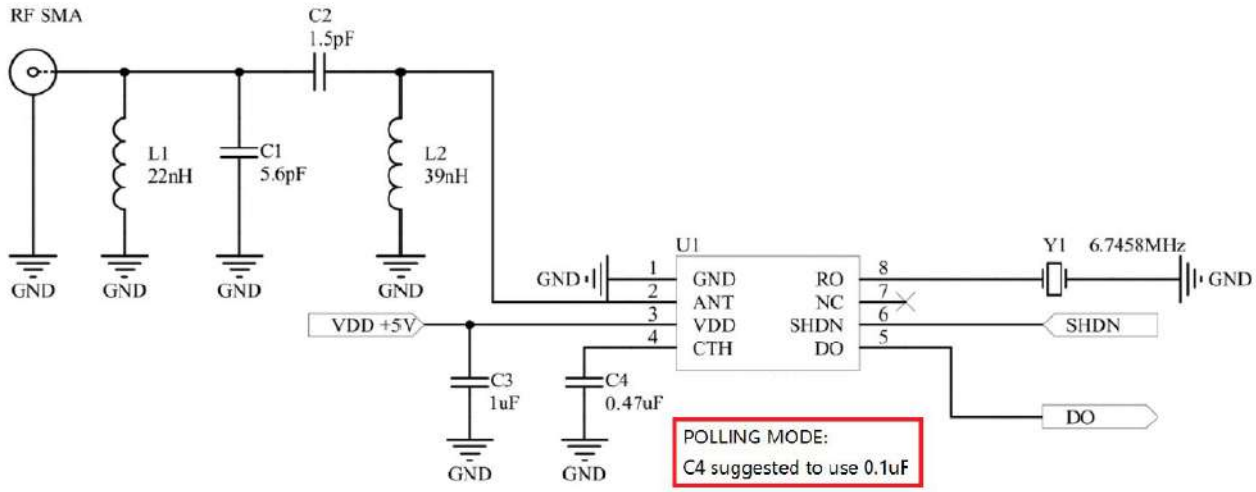
Pin Configuration



Pin Description

Pin	Name	I/O	Function
1	GND	GND	Ground
2	ANT	I	RF Input
3	VDD	POWER	Power Supply
4	CTH	I	Slicing Level Capacitor
5	DO	O	Data Output
6	SHDN	I	Shut Down(Low Level Enable)
7	NC		Not Connected
8	RO	I	Reference Crystal Oscillator

Typical Application



CY310 433.92MHz, 1kHz Baud Rate Application Circuit

CY310 requires only one components to operate: one capacitor (CTH) and the reference frequency device, usually a quartz crystal. Additional five components may be used to improve performance. These are: power supply decoupling capacitor, two components for the matching network, and two components for the pre-selector band pass filter.

Absolute Maximum Ratings

Supply Voltage 7V
Input Voltage 7V
ESD Rating .....Note 1
Storage Temperature Range .....-65° C to 150° C
Junction Temperature .....150° C
Lead Temperature (soldering, 10sec.) .....260° C

Operating Ratings

Supply Voltage .....1.8V to 5.5V
Input Voltage (Max) 5.5V
Ambient Temperature (TA) .....-40° C to 85° C

Electrical Characteristics

Unless otherwise noted, VDD = 5V, CTH = 0.1μF (for CY310), 1Kbps data rate (Manchester encoded, BER =10E-2), all test at TA = 25° C.

Power Supply

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{CC}	Supply Current	f_{RX} = 315MHz		4.9		mA
		f_{RX} = 433.92MHz		5.4		mA
I_{OFF}	Shut Down Current	SHDN = High		1		μA

Receiver

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{RX}	Frequency Input Range		300 to 450			MHz
$P_{IN,MAX}$	Maximum Input Power				10	dBm
P_{SENS}	Receiver Sensitivity (Note 2)	f_{RX} = 315MHz		-114		dBm
		f_{RX} = 433.92MHz		-114		dBm
	Image Rejection	f_{RX} = 315MHz		30		dB
		f_{RX} = 433.92MHz		30		dB
f_{IF}	1st IF Center Frequency	f_{RX} = 315MHz		0.86		MHz
		f_{RX} = 433.92MHz		1.2		MHz
	IF Bandwidth	f_{RX} = 315MHz		350		kHz
		f_{RX} = 433.92MHz		600		kHz
	Receive ModulationDuty Cycle	Note 3	20		80	%

Reference Oscillator

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{OSC}	Frequency	f_{RX} = 315MHz		4.897		MHz
		f_{RX} = 433.92MHz		6.7458		MHz
V_{OSC}	Reference Oscillator Bias Voltage			1.15		V
	Reference Oscillator Input Range		0.2		1.5	V_{PP}
I_{OSC}	Source Current	V(RO) = 0V		3.5		µA

DO Drive

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
	DO pin Output Current	Source @ 0.8VDD		260		µA
		Sink @ 0.2 VDD		600		µA
T_{RISE}	Output Rise and Fall Times	C_L = 15pF, pin DO, 10-90%		2		µsec
T_{FALL}				2		µsec

Note 1: Device is ESD sensitive. Use appropriate ESD precautions. Exceeding the absolute maximum rating may damage the device.

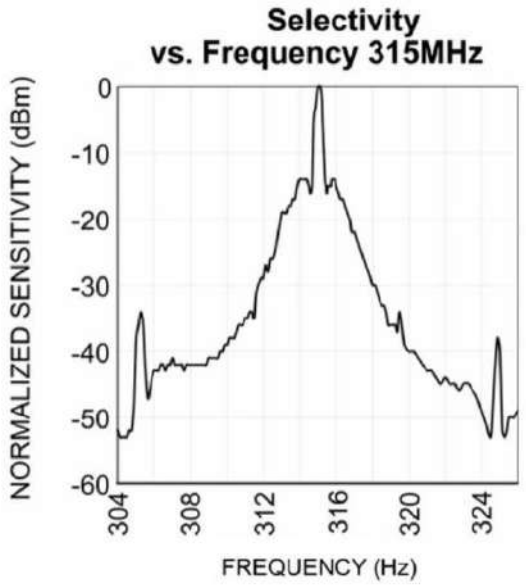
Note 2: Sensitivity is defined as the average signal level measured at the input necessary to achieve 10-2 BER (bit error rate). The input signal is defined as a return-to-zero (RZ) waveform with 50% average duty cycle (Manchester encoded) at a data rate of 1kbps.

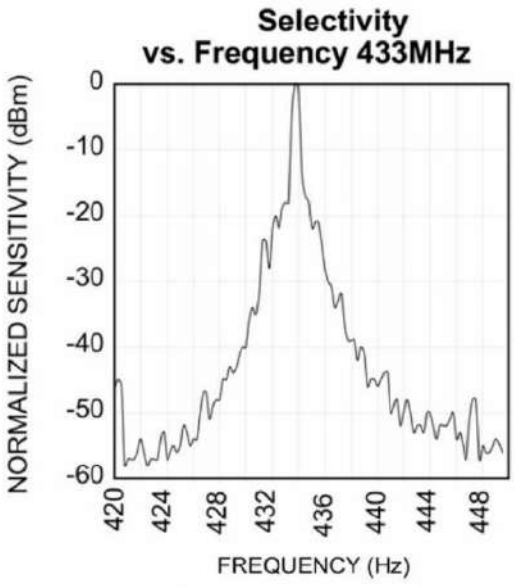
Note 3: When data burst does not contain preamble, duty cycle is defined as total duty cycle, including any “quiet” time between data bursts. When data bursts contain preamble sufficient to charge the slice level on capacitor CTH, then duty cycle is the effective duty cycle of the burst alone.

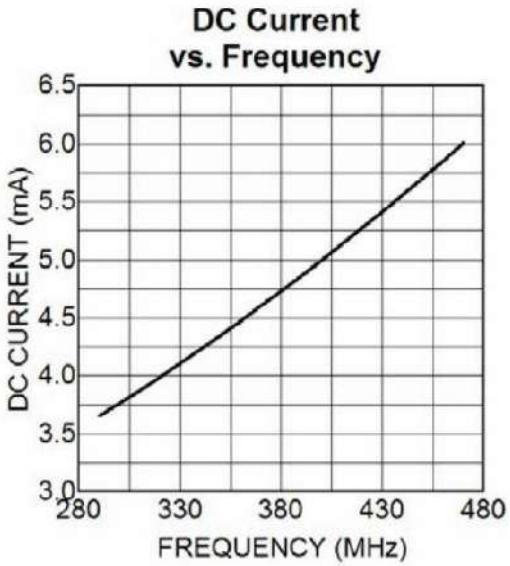
[For example, 100msec burst with 50% duty cycle, and 100msec “quiet” time between bursts. If burst includes preamble, duty cycle is TON/(TON + TOFF) = 50%; without preamble, duty cycle is TON/(TON + TOFF + TQUIET) = 50msec/(200msec) = 25%. TON is the (Average number of 1’s/burst) × bit time, and TOFF = TBURST–TON.]

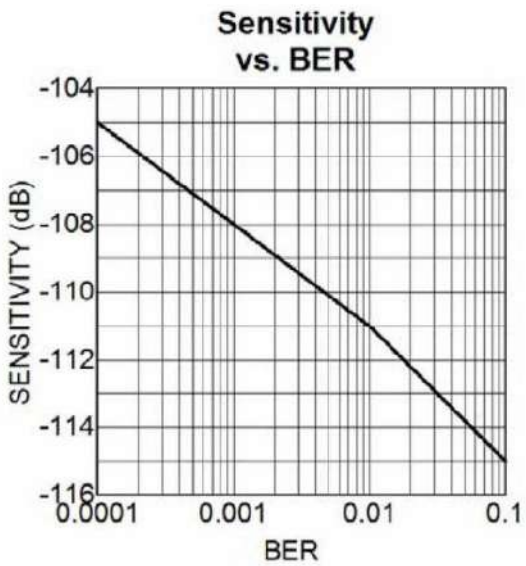
Typical Characteristics

Unless otherwise noted, VDD = 5V, CTH = 0.1µF (for CY310), 1Kbps data rate (Manchester encoded, BER =10E-2), all test at TA = 25° C.









Functional Diagram

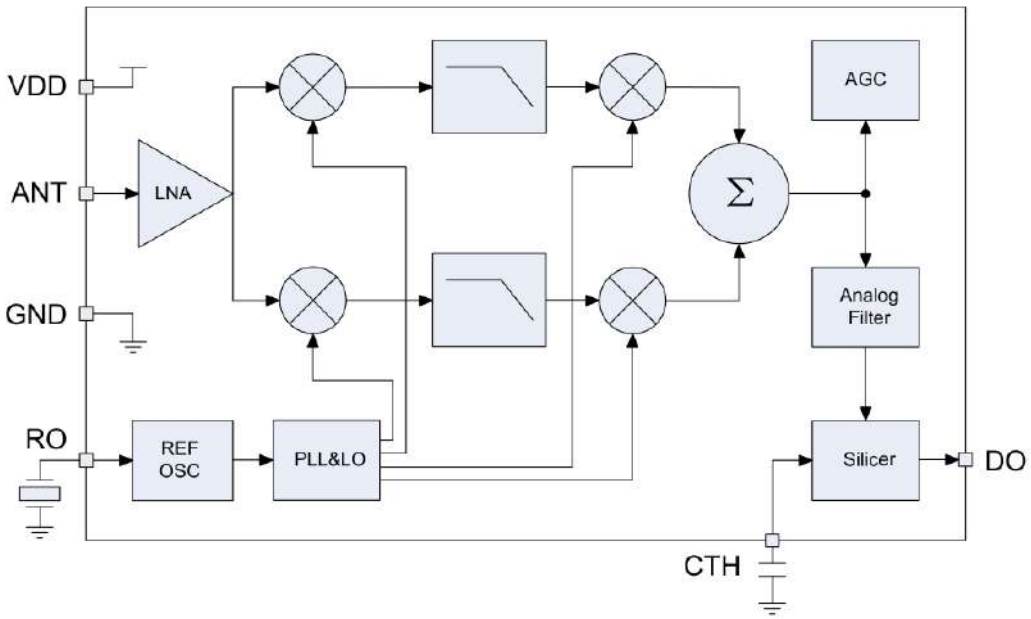


Figure 1 Simplified Block Diagram

Functional Description

Figure 1 Simplified Block Diagram illustrates the basic structure of the CY310. The CTH pin with capacitor is necessary for CY310. It is composed of five modules; Low Noise Amplifier, Weaver architecture receiver, the Slicer, Auto Gain Control and Reference and Control Logics.

LNA

The RF input signal is AC-coupled into the gate circuit of the grounded source LNA input stage. The LNA uses a Cascoded NMOS structure circuit, and the output is converted to differential signals for next stage mixers.

Weaver Receiver

The LNA output signals are first mixed with quadrature phases of the local oscillator signal. After filtering both mixer output with a low-pass filter, the output signals are mixed again by another set of mixing operation in both signal paths, the sum of the two final signals cancels the image band to yield the desired signal, while the subtraction removes the desired signal and selects the image band.

Slicer

The signal prior to slicer is still linear demodulated AM. Data slicer converts this signal into digital “1” and “0” by comparing with the threshold voltage built up on the CTH capacitor. This threshold is determined by detecting the positive and negative peaks of the data signal and storing the mean value. Slicing threshold is at 50%. After the slicer, the signal is now digital

OOK data. During long periods of “0” or no data period, threshold voltage on the CTH capacitor may be very low. Large random noise spikes during this time may cause erroneous “1” at DO pin

Reference Oscillator

The reference oscillator in the CY310 uses a basic Colpitts crystal oscillator configuration with MOS transconductor to provide negative resistance. The RO pin external capacitor is integrated inside CY310. User only needs to connect reference oscillation crystal.

Reference oscillator crystal frequency can be calculated: $F_{OSC} = F_{RF}/(64.5 – 1.76/10)$

For 433.92 MHz, FOSC = 6.7458 MHz.

Evaluation Board

Figure 2, 3 and 4 show the top, bottom and top solder layers of CY310 @433.92MHz application board.

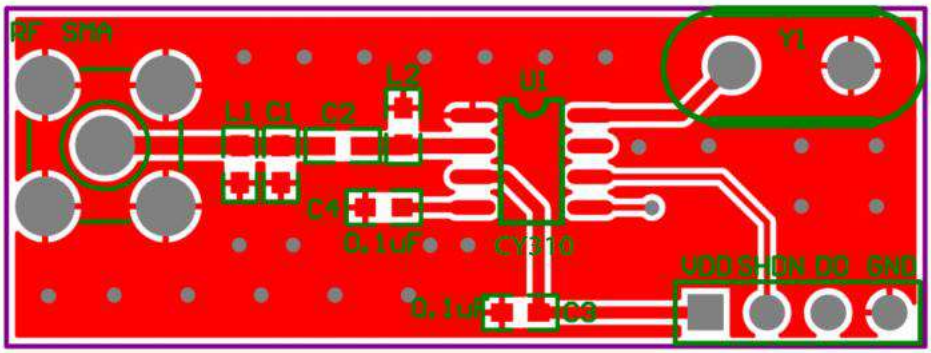


Figure 2 Top Layer

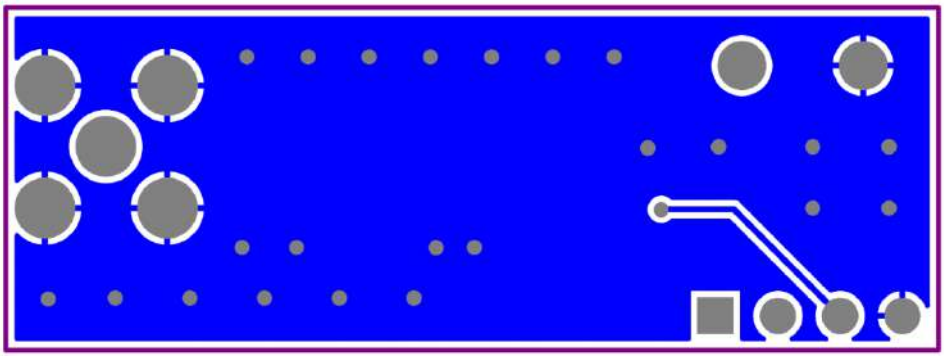


Figure 3 Bottom Layer

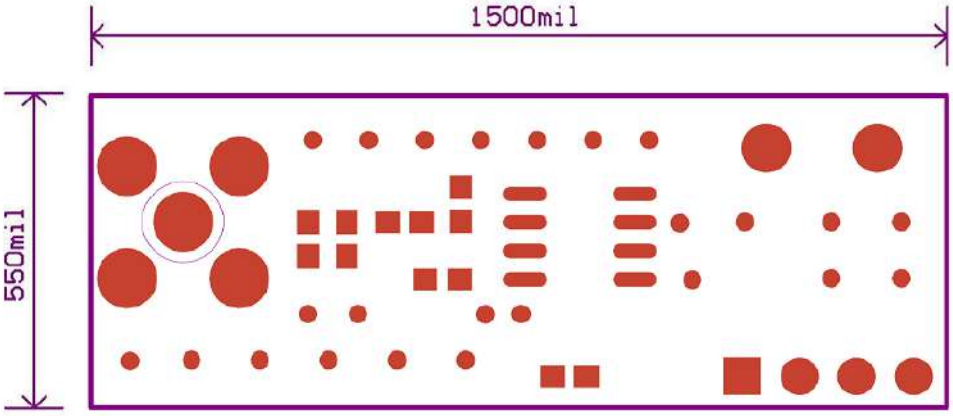


Figure 4 Top Solder Layer with Dimensions

Board Bill of Materials

Below form shows the bill of CY310 @315MHz application board.

Footprint	Comment	Designator	Description	Quantity
0603-STD	6.8pF	C1	Capacitor	1
0603-STD	1.8pF	C2	Capacitor	1
0603-STD	1μF	C3	Capacitor	1
0603-STD	0.47μF	C4	Capacitor	1
0603-STD	39nH	L1	Inductor	1
0603-STD	68nH	L2	Inductor	1
SMA-KWE	RF SMA	P1	SMA Connector	1
HDR1X4	Header 3	P2	Header, 4-Pin	1
SOP-8	CY310	U1	SINOTA	1
XTAL-HC49S	4.8970MHz	Y1	Crystal Oscillator	1

Below form shows the bill of CY310 @433.92MHz application board.

Footprint	Comment	Designator	Description	Quantity
0603-STD	5.6pF	C1	Capacitor	1
0603-STD	1.5pF	C2	Capacitor	1
0603-STD	1μF	C3	Capacitor	1
0603-STD	0.47uF	C4	Capacitor	1
0603-STD	22nH	L1	Inductor	1
0603-STD	39nH	L2	Inductor	1
SMA-KWE	RF SMA	P1	SMA Connector	1
HDR1X4	Header 4	P2	Header, 4-Pin	1
SOP-8	CY310	U1	SINOTA	1
XTAL-HC49S	6.7458MHz	Y1	Crystal Oscillator	1

Package Description

SOP-8 Package Outline Dimensions shown in millimeters and (inches)