+15kV ESD Protected, 500kbps Data Rate Polarity Adaptation RS-485

CYP485N

General Description

The CYP485N is a half-duplex high speed transceiver for RS-485 communication. IC contains one driver and one receiver, it has adaptive function.

The CYP485N has a fail-safe circuit ， ensure logical high level of receiver output when receiver input is open or short.

The CYP485N receiver has 1/8 unit load input impedance, allows up to 256 devices can be attached to the bus.

Features

- I/O pin ESD protection: +15kV HBM IEC 61000-4-2
  Other pins have level 3 ESD protection: >+8kV HBM
- Fractional unit load allows up to 256 devices on the bus
- Adaptive connection function: reverse connection communication of communication ports A and B is realized, polarity recognition time is 78ms
- Operating voltage: +5V (Typical.)
- Low current shutdown mode operating current: 1nA
- Current limiting and thermal turn-off function can be used for driver overload protection
- SOP8 package

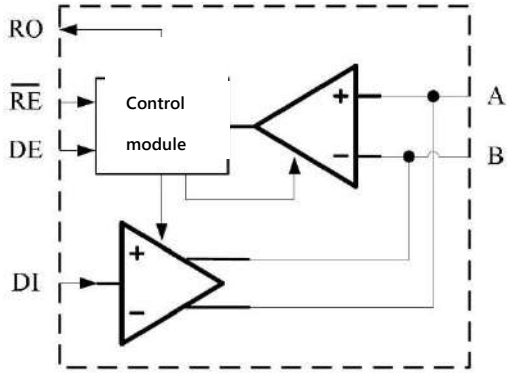
Applications

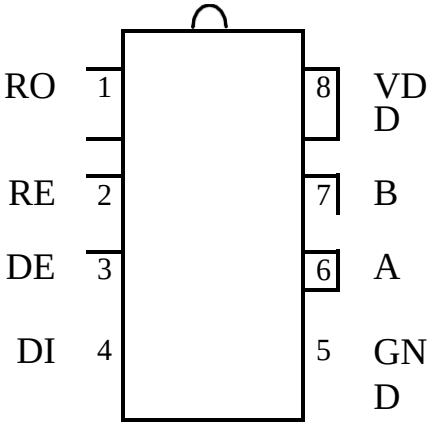
- Intelligent instrument
- Industrial process control
- Building automation network
- Motor control

Order specification

Part No	Package	Manner of Packing	Devices per bag/reel
CYP485N	SOP8	Reel	2500

Block Diagram and Pin Arrangement Diagram





Pin Assignment

Pin No.	Pin Name	Description	I/O
1	RO	Receiver output：If A is connected to bus A,If A-B≥0.1V，RO will be high； If A-B≤-0.1V，RO will be low； If A and B are open or shorted，RO will be high. If A is connected to bus B, RO will on the contrary.	O
2	$\overline{RE}$	Receiver output enable: RO is enabled when $\overline{RE}$ is low； RO is high impedance when $\overline{RE}$ is high.	I
3	DE	Driver output enable： The driver outputs, A and B are enabled by bringing DE high. They are high impedance when DE is low.	I
4	DI	Driver input: If A is connected to bus A, A low on DI forces output A low and output B high. Similarly, a high on DI forces output A high and output B low. If A is connected to bus B, A and B will on the contrary.	I
5	GND	Ground	
6	A	Receiver input and driver output	I/O
7	B	Receiver input and driver output	I/O
8	VDD	Supply voltage	

Functional Description

The CYP485N is a half-duplex high speed transceiver for RS-485 communication. IC contains one driver and one receiver. It has adaptive function, AB terminal reverse connection can also communicate normally. The CYP485N receiver has 1/8 unit load input impedance, allows up to 256 devices can be attached to the bus.

Description of circuit function control

Control pin		Function
$\overline{RE}$	DE	
L	X	Receiver mode
X	H	Driver mode

Receiver Truth Table

Input			Output
$\overline{RE}$	DE	A - B	RO
L	X	≥0.1V	H
L	X	≤-0.1V	L
L	X	Open/shorted	H
H	H	X	Z
H	L	X	Z

Driver Truth Table

Input			Output	
$\overline{RE}$	DE	DI	B	A
X	H	H	L	H
X	H	L	H	L
L	L	X	Z	Z
H	L	X	Z	

Absolute Maximum Ratings

Unless specified otherwise, Tamb= 25℃

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3~7	V
Input / Output Voltage	V_{IN}/V_{OUT}	GND-0.3~V_{DD}+0.3	V
A/B Input / Output Voltage	$V_{INA/B}/V_{OUTA/B}$	-13~15	V
Operating Temperature	T_{amb}	-40~85	℃
Storage Temperature	T_{stg}	-65~150	℃

DC Electrical Characteristics

Unless specified otherwise, VDD=5V±5%, Tamb= 25℃

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating voltage	V_{CC}		4.5		5.5	V
Driver						
Differential driver output	V_{OD1}	No load			5	V
Differential driver output	V_{OD2}	R=50Ω(1)	2.0	3.5		V
		R=27Ω(1)	1.5	2.7		V
Change in magnitude of driver differential output voltage for complementary output states	ΔV_{OD}	R=50Ω or 27Ω(1)		0.01	0.2	V
Driver common-mode output voltage	V_{OC}	R=50Ω or 27Ω(1)		2.2		V
Change in magnitude of driver common-mode output voltage for complementary output states	ΔV_{OC}	R=50Ω or 27Ω(1)		0.01	0.2	V
Input high voltage	V_{IH1}	DE、RE、DI	2.0			V
Input low voltage	V_{IL1}	DE、RE、DI			0.8	V
Input current	I_{IN1}	DE、RE、DI	-2		2	μA
Input current (A, B)	I_{IN2}	DE=GND, V_{DD} =GND or 5.25V, Vin=12V			75	μA
		DE=GND, V_{DD} =GND or 5.25V, Vin=-7V			-75	μA
Driver short-circuit current	I_{OD1}	-7V≤V_{OUT}≤V_{DD}	-250			mA
		0V≤V_{OUT}≤12V			250	mA
		0V≤V_{OUT}≤V_{DD}	±25			mA
Receiver						
Differential threshold voltage	V_{TH}	-7V≤V_{CM}≤12V	-100	-50	100	mV
input hysteresis voltage	ΔV_{TH}			25		mV
output high voltage	V_{OH}	I_O=-4mA，V_{ID}=-50mV	4.5			V
output low voltage	V_{OL}	I_O=4mA，V_{ID}=-200mV			0.2	V
3-state(high impedance) output current at receiver	I_{OZR}	0.4V≤V_O≤2.4V			±1	μA
input resistance	R_{IN}	-7V≤V_{CM}≤12V	96			kΩ
Receiver short-circuit current	I_{OSR}	0V≤V_{RO}≤V_{DD}	±7		±95	mA

Supply Current	I_{CC}	No load, $\overline{RE}$=DI =GND or V_{DD}	DE=V_{DD}		520	600	μA
			DE=GND		430	600	μA
Polarity Discrimination Time	Tdtect				78		ms

Transmission characteristics

Unless specified otherwise，VDD=5V±5%，Tamb= 25℃

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Driver Input to Output	t_{DPLH}	R_{DIFF}=54Ω， C_{L1}=C_{L2} =100pF(2)		34	60	ns
Driver Input to Output	t_{DPHL}	R_{DIFF}=54Ω， C_{L1}=C_{L2} =100pF(2)		34	60	ns
$\|t_{DPLH}-t_{DPHL}\|$	t_{DSKEW}	R_{DIFF}=54Ω， CL1=CL2=100pF(2)		-2.5	±10	ns
Driver Rise or Fall Time	t_{DR},t_{DF}	R_{DIFF}=54Ω， C_{L1}=C_{L2} =100pF(2)		14	25	ns
Maximum Data Rate	f_{MAX}		500			kbps
Driver Enable to Output High	t_{DZH}	C_L=100pF，S2 closed(3)			150	ns
Driver Enable to Output Low	t_{DZL}	C_L=100pF，S1 closed(3)			150	ns
Driver Disable Time from Low	t_{DLZ}	C_L=15pF，S1 closed(3)			100	ns
Driver Disable Time from Low	t_{DHZ}	C_L=15pF，S2 closed(3)			100	ns
Receiver Input to Output	t_{RPLH}	$\|V_{ID}\|$≥2.0V Rise or Fall Time≤15ns(4)		127	200	ns
Receiver Input to Output	t_{RPHL}			127	200	ns
$\|t_{RPLH}-t_{RPHL}\|$	t_{RSKD}	$\|V_{ID}\|$≥2.0V Rise or Fall Time≤15ns(4)		3	±30	ns
Receiver Enable to Output Low	t_{RZL}	C_L=100pF，S1 closed(5)		20	50	ns
Receiver Enable to Output High	t_{RZH}	C_L=100pF，S2 closed(5)		20	50	ns
Receiver Disable Time from Low	t_{RLZ}	C_L=100pF，S1 closed(5)		20	50	ns
Receiver Disable Time from High	t_{RHZ}	C_L=100pF，S2 closed(5)		20	50	ns

Note：

(1) Test circuit is shown in Figure 1

(2) Test circuit is shown in Figure 2

(3) Test circuit is shown in Figure 3

(4) Test circuit is shown in Figure 4

(5) Test circuit is shown in Figure 5

Test Circuit

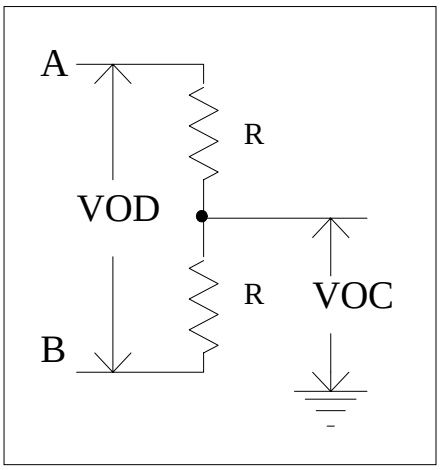


Figure 1 Driver DC Test Circuit

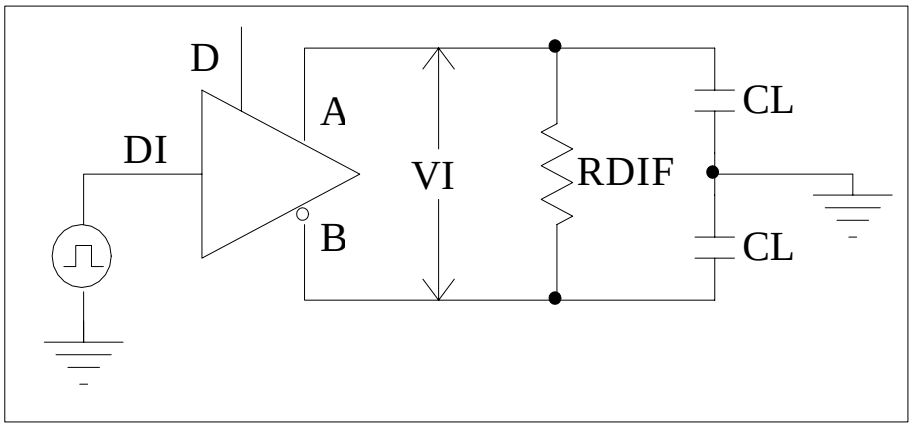


Figure 2 Driver Timing Test Circuit

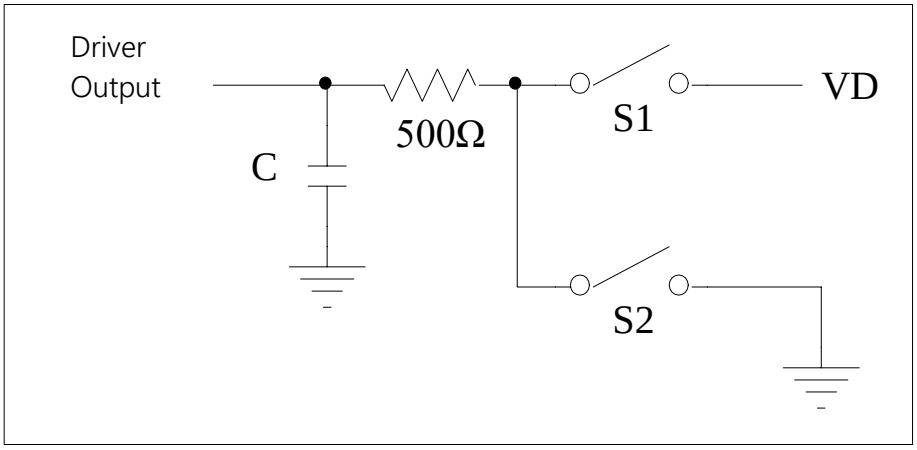


Figure 3 Driver Enable/Invalid Timing Test Circuit

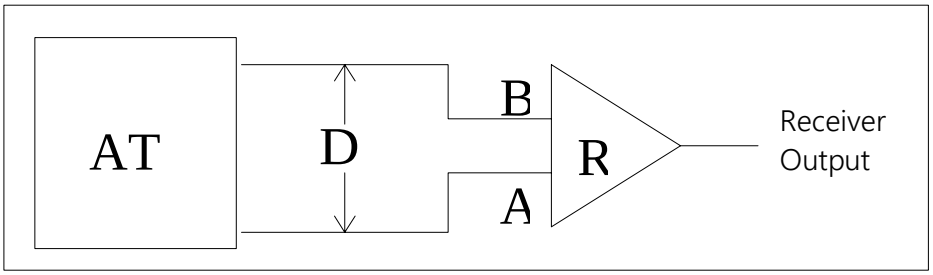


Figure 4 Receiver Propagation Delay Test Circuit

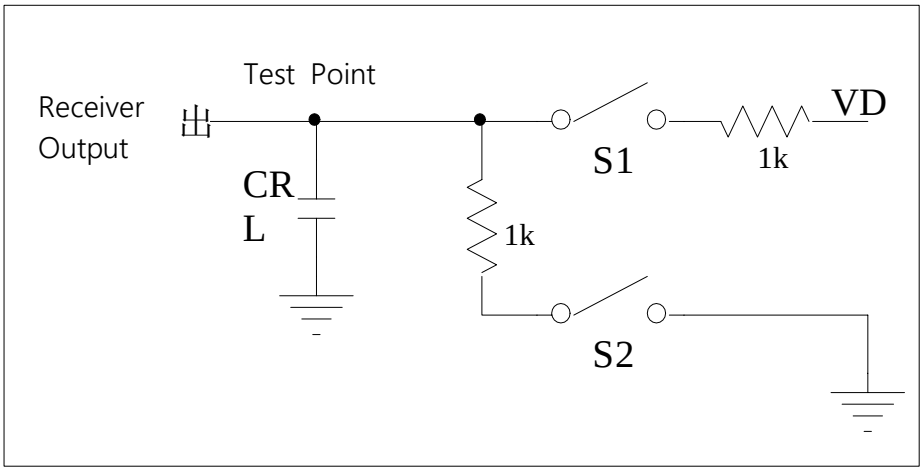


Figure 5 Receiver Enable/Invalid Timing Test Circuit

Application Circuits

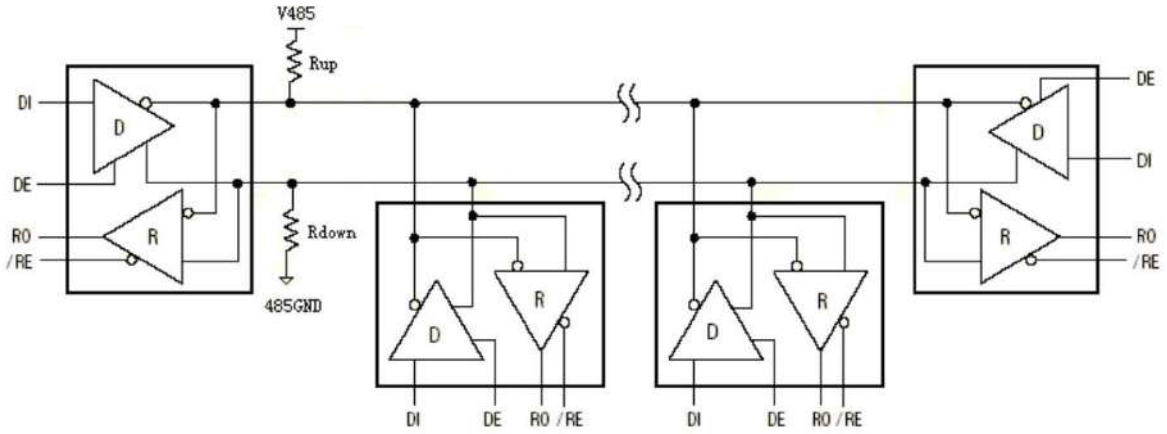


Figure 6 Typical Application Chart

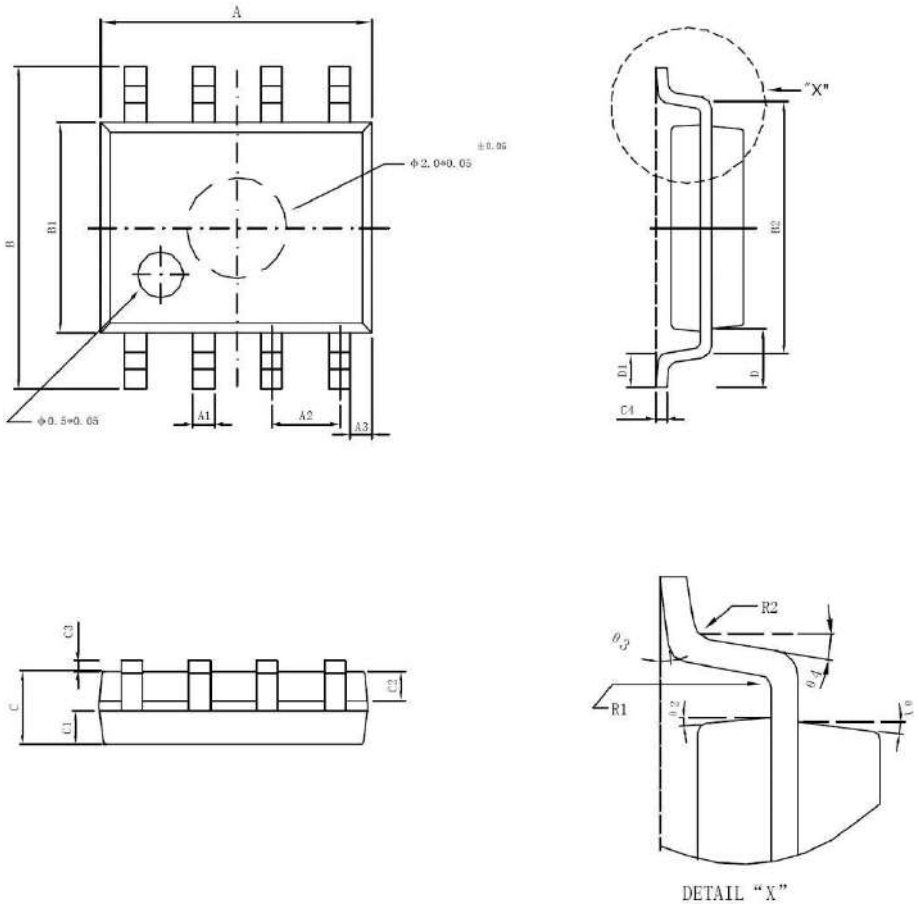
In an RS-485 communication network, an RS-485 transceiver as a host (such as a concentrator) is connected to an RS-485 transceiver as a slave (such as a smart electricity meter) through two buses. In a traditional RS-485 system, the polarity of the two buses needs to be distinguished, and all the RS-485 transceiver bus ports in the system need to match the polarity.

The CYP485N has a built-in polarity judgment circuit. After being powered on, the CYP485N automatically detects the system bus polarity. After 78ms, the CYP485N automatically adjusts the port polarity to match the system bus polarity. Figure 6 shows A typical polarity adaptive network application circuit. In this system, ports A and B of the host need to be connected with appropriate pull-up and pull-down resistors (for example, 1K resistor) according to the situation, while ports A and B of the slave cannot be connected with pull-up and pull-down resistors, complete the polarity discrimination in the acceptance state.

After the time of polarity discrimination, polarity correction is completed. The state of the bus polarity is locked in the transceiver and held for subsequent data transfer. Data string duration of consecutive "0" or "1" exceeding the polarity determination time may accidentally trigger false polarity correction and should be avoided.

In the CYP485N polarity adaptive bus, it is recommended that the host and slave all adopt polarity adaptive chip for communication, and the mixed use of heteropolarity and polarity adaptive is not recommended.

Package Information（SOP8）



Symbol	Min.（mm）	Max.（mm）	Symbol	Min.（mm）	Max.（mm）
A	4.95	5.15	**C3**	0.10	0.20
A1	0.37	0.47	**C4**	0.20TYP	
A2	1.27TYP		**D**	1.05TYP	
A3	0.41TYP		**D1**	0.50TYP	
B	5.80	6.20	**R1**	0.07TYP	
B1	3.80	4.00	**R2**	0.07TYP	
B2	5.0TYP		**θ1**	17°TYP	
C	1.30	1.50	**θ2**	13°TYP	
C1	0.55	0.65	**θ3**	4°TYP	
C2	0.55	0.65	**θ4**	12°TYP	

Special Instructions

The company reserves the right of final interpretation of this specification.

Version Change Description

Version：V1.3	Author：Yangyang	Time：2021.8.12
Modify the record：		
1. Re-typesetting the manual and checking some data		
Version：V1.4	Author：Yangyang	Time：2022.5.12
Modify the record：		
1. Add precautions for the use of polarity adaptive		
Version：V1.5	Author：Yangyang	Time：2022.10.17
Modify the record：		
1. Deleting the description and parameters of slew-rate-limited		